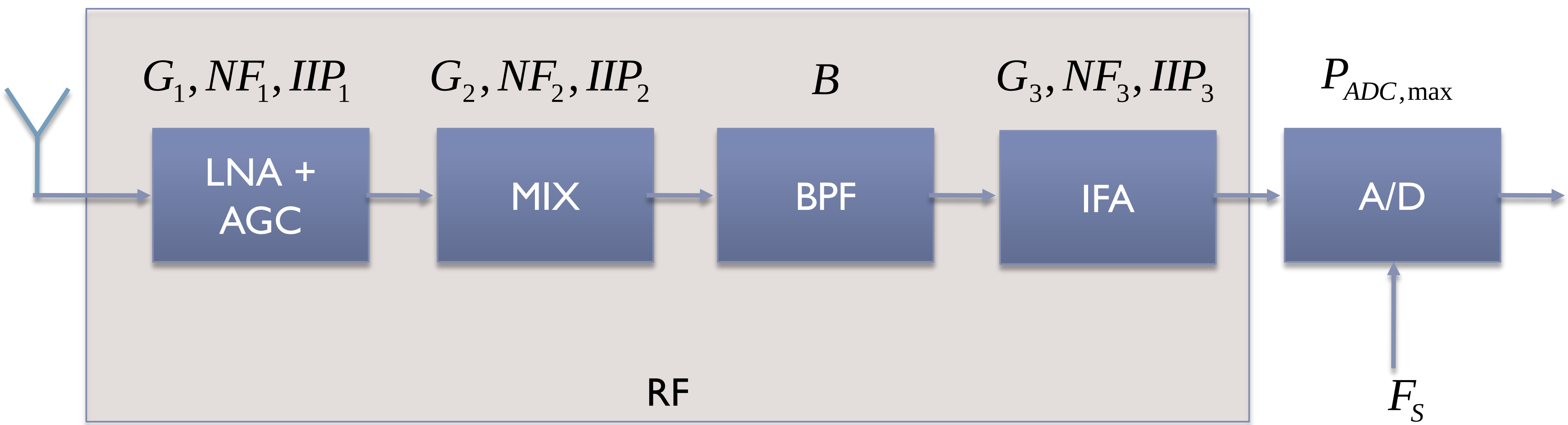
Chapter 3. DFE - Outline

- General Aspects
- DFE Tx
- **DFE Rx**

General diagram of a RR

- Classical diagram of the superheterodyne receiver



Implementing a SDR

- Physical layer constraints:
  - Ensuring the quality of the link
    - Minimum SNR for a given modulation
  - Avoiding the saturation of the receiver
    - P_{max} at the input of the receiver
    - P_{max} at the input of the A/D converter
- Calculated parameters
  - Resulted dynamic range
  - A/D converter resolution
  - Gain on the receive chain
  - Variation range of the AGC

Perturbations in a RR

- Interferences
  - Perturbations that reached the band of interest
- Noise in the RR
  - Noise captured from the antenna and processed by the receiver signal processing chain
- Quantization noise in the A/D converter
  - Approximation of the analog signal

Noise in the RR

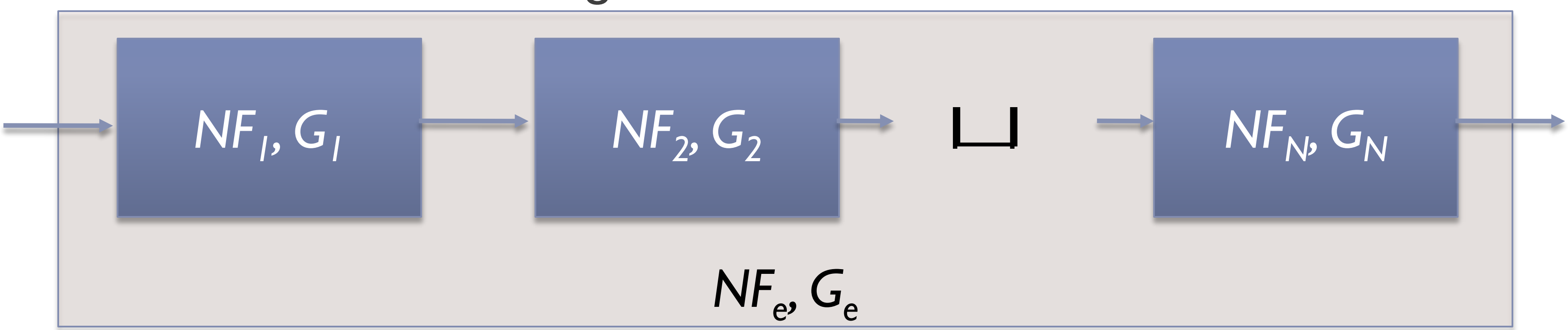
- Noise figure (NF)

$$S_o = GS_i$$

$$N_o = G \cdot NF \cdot N_i$$

$$\left(\frac{S_o}{N_o}\right) = \frac{1}{NF}\left(\frac{S_i}{N_i}\right)$$

- Noise figure of a chain of blocks

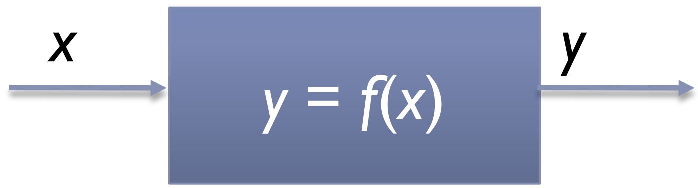


$$NF_e = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_N - 1}{G_1 \ldots G_{N-1}}$$

$$G_e = G_1 \ldots G_{N-1}$$

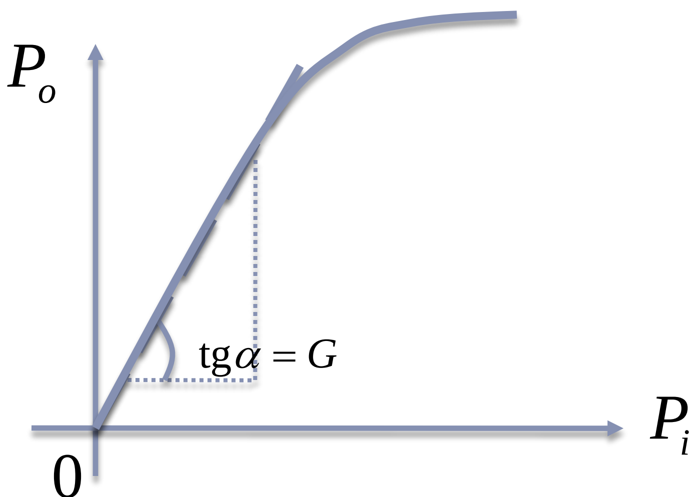
Amplifier distortions

- Cause: circuit nonlinearities

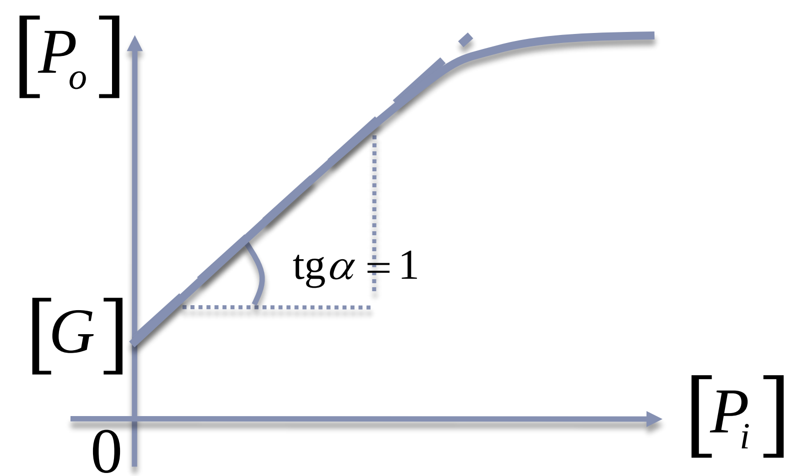


Ideal

$$P_o = GP_i$$



$$[P_o] = [G] + [P_i]$$



Intermodulation products

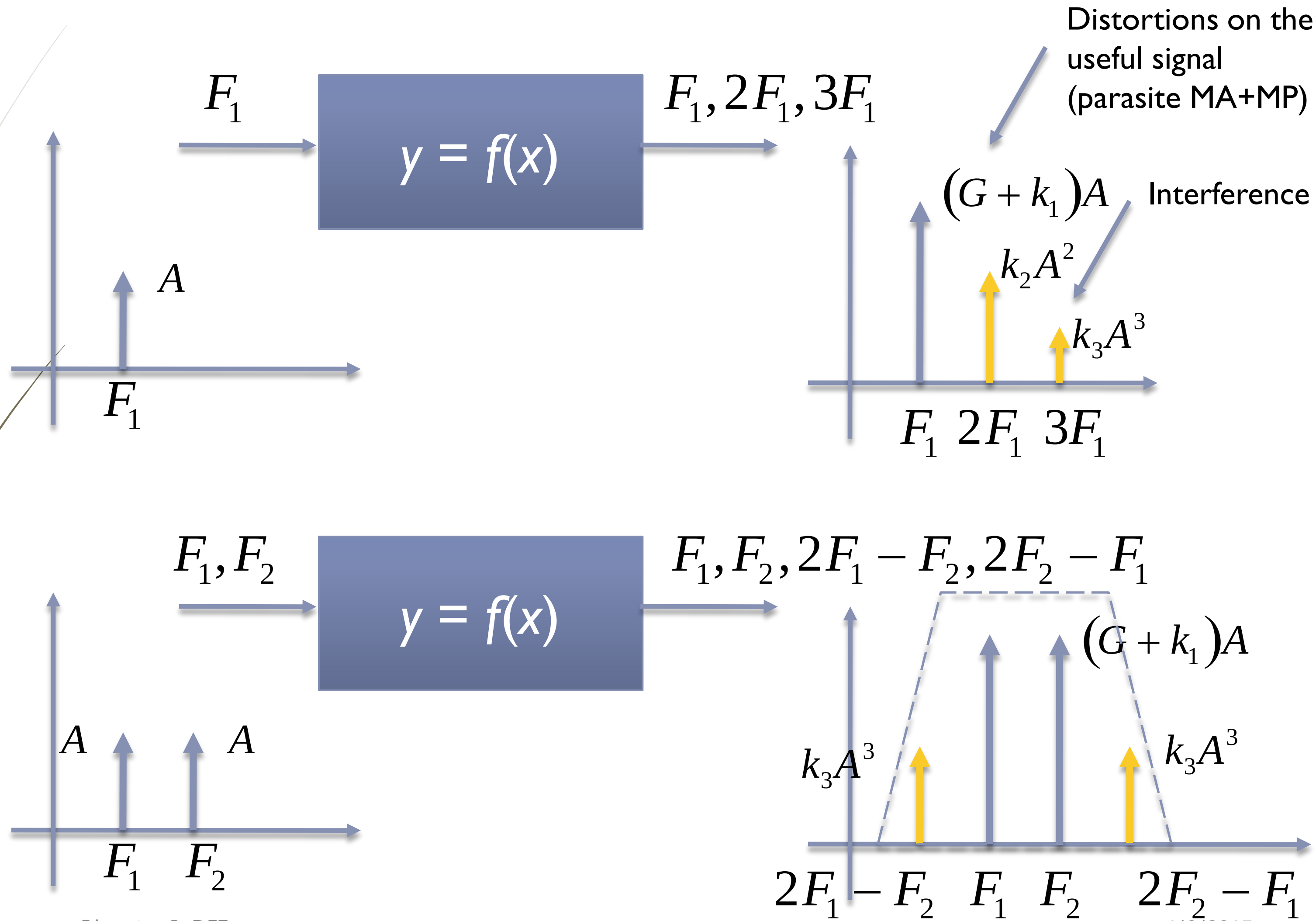
$$y = a_1 x + a_2 x^2 + a_3 x^3 + \ldots$$

Ideal → $F_o = F_{i,k}$

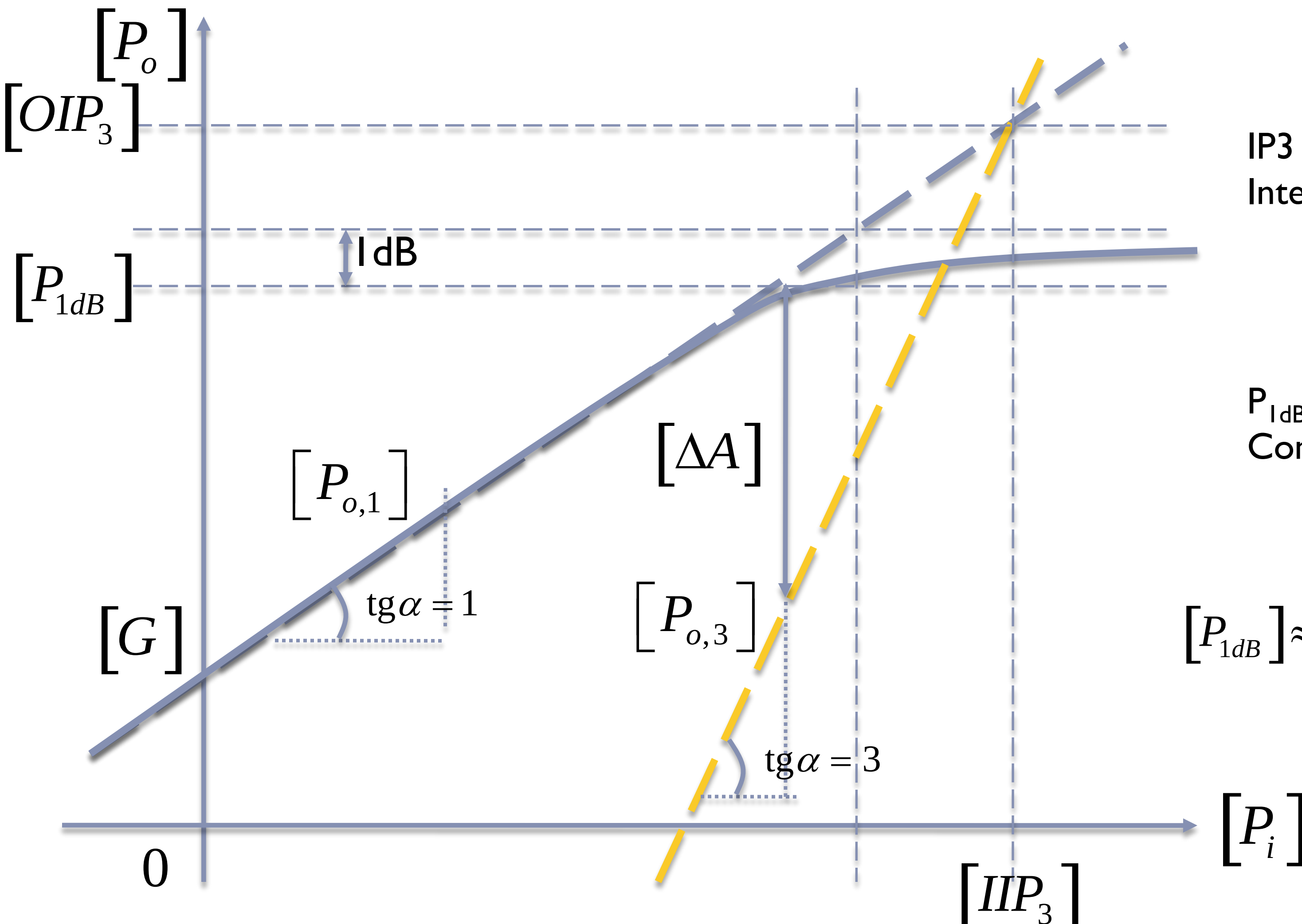
2nd order distortions → $F_o = \sum_k N_k F_{i,k} \;, \sum_k |N_k| = 2$

3rd order distortions → $F_o = \sum_k N_k F_{i,k} \;, \sum_k |N_k| = 3$

Intermodulation products (2)



Nonlinearities effects



IP3 = 3rd Order Interception Point

P_{1dB} =1dB Compression Point

$$[P_{1dB}] \approx [OIP_3] - 10dB$$

Interception point

- Interception point for a chain of blocks:

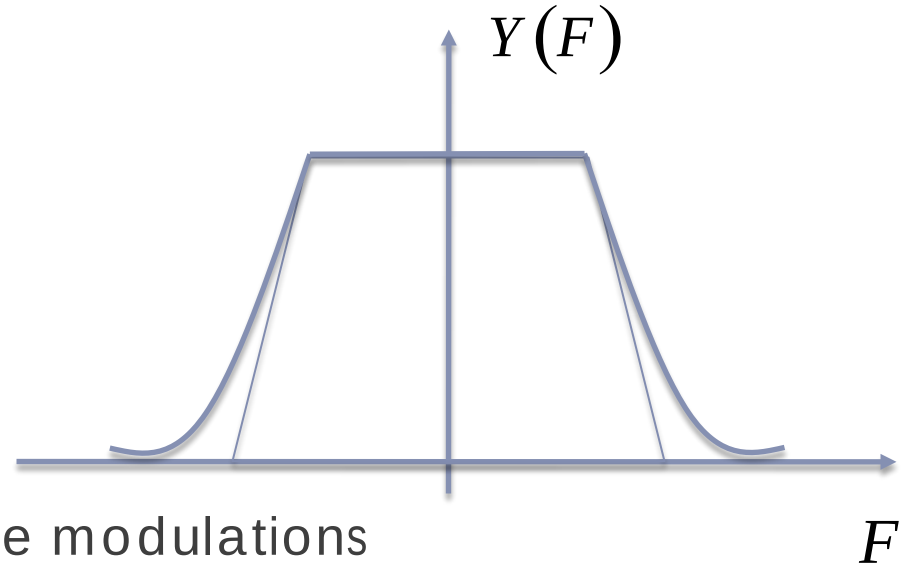
$$OIP_{3,e} = \frac{1}{\frac{1}{OIP_{3,1}G_2G_3\ldots G_N} + \frac{1}{OIP_{3,2}G_3\ldots G_N} + \ldots + \frac{1}{OIP_{3,N-1}G_N} + \frac{1}{OIP_{3,N}}}$$

$$[OIP_3] = [P_{o,1}] + \frac{[\Delta A]}{2}$$

$$[IIP_3] = [P_{i,1}] + \frac{[\Delta A]}{2}$$

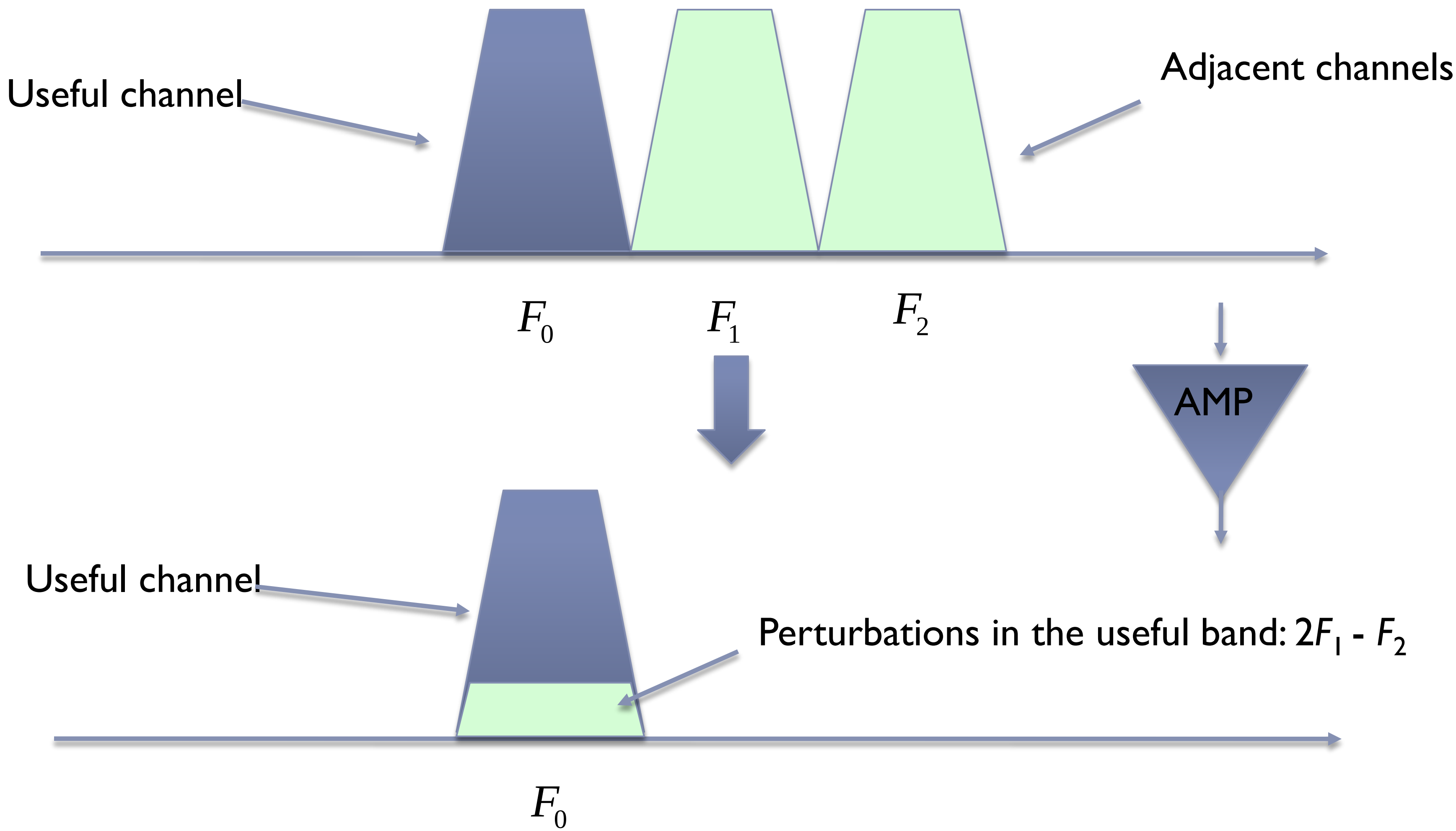
Effects on the transmitter

- Ideal: $y(t) = Gx(t)$
- Real: $y(t) = G(x(t))x(t)e^{j\varphi(t)}$



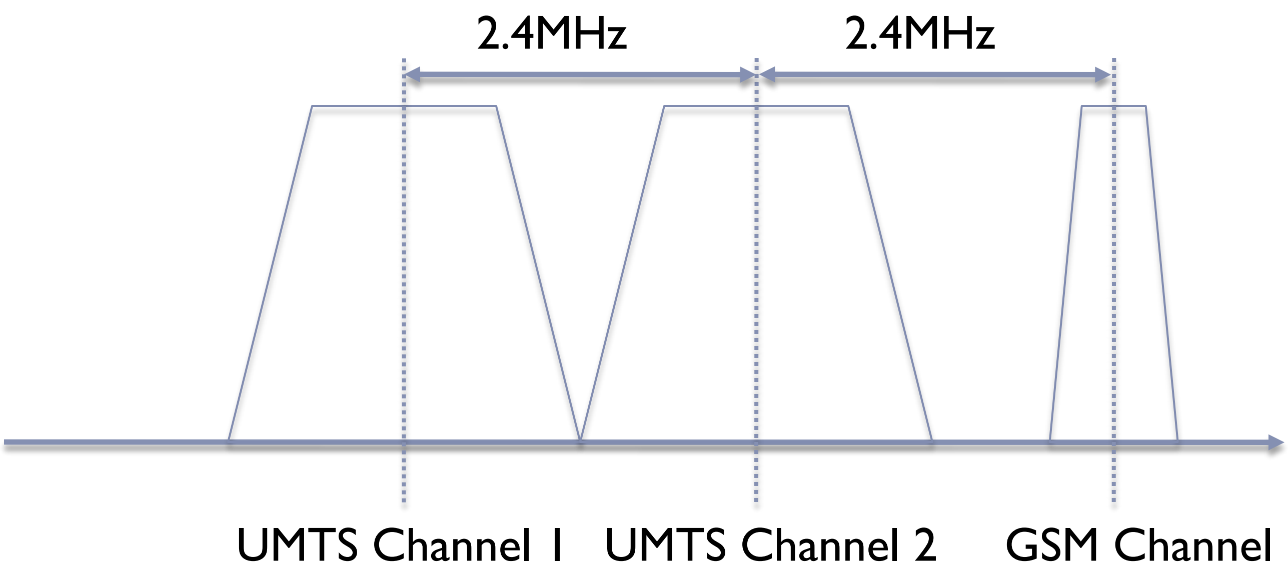
- Parasite amplitude and phase modulations
- Artificial growth of signal bandwidth
  - Possible violation of spectral masks
- The amplifier has to be used far away from the 1dB compression point

Effects on the receiver



How is the necessary IIP determined?

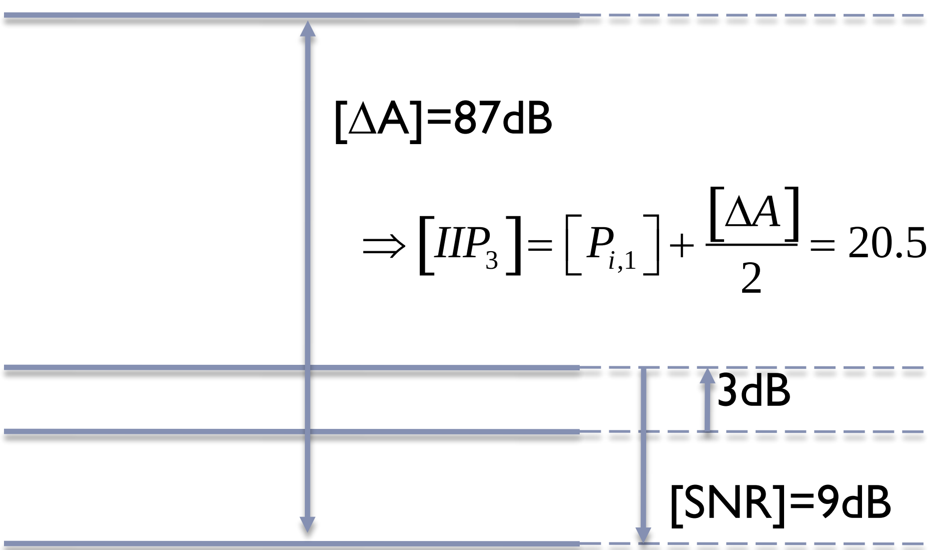
- Example:
  - Useful signal: GSM
  - Perturbation signals: UMTS channels spaced at 2.4 MHz



$B \approx 5MHz$ $B \approx 5MHz$ $B \approx 200kHz$

How is the necessary IIP determined? (2)

- Example:
  - Receiver with gain $[G] = 20dB$
- At 2.4 MHz, the maximum admitted interference level is: $[P_{i,1}] = -23dBm$



The maximum admitted interference level at the receiver input= -23dBm

$$\Rightarrow [IIP_3] = [P_{i,1}] + \frac{[\Delta A]}{2} = 20.5dBm$$

$$\Rightarrow [OIP_3] = [IIP_3] + [G] = 40.5dBm$$

Signal level= -101dBm

Reference level = -104dBm

The maximum admitted interference level at the receiver output = -110dBm

The A/D Converter

- Is responsible for:
  - Sampling

$$F_S \geq 2F_{\max}$$

  - Quantization

$$\left[SNR_c\right] = 1.76dB + 6.02b + 10\lg\left(\frac{F_S}{2F_{\max}}\right)$$

Number of bits (Converter resolution)

Oversampling gain

  - The resolution is chosen so that: $SNR_c \leq SNR_o$

The A/D Converter (2)

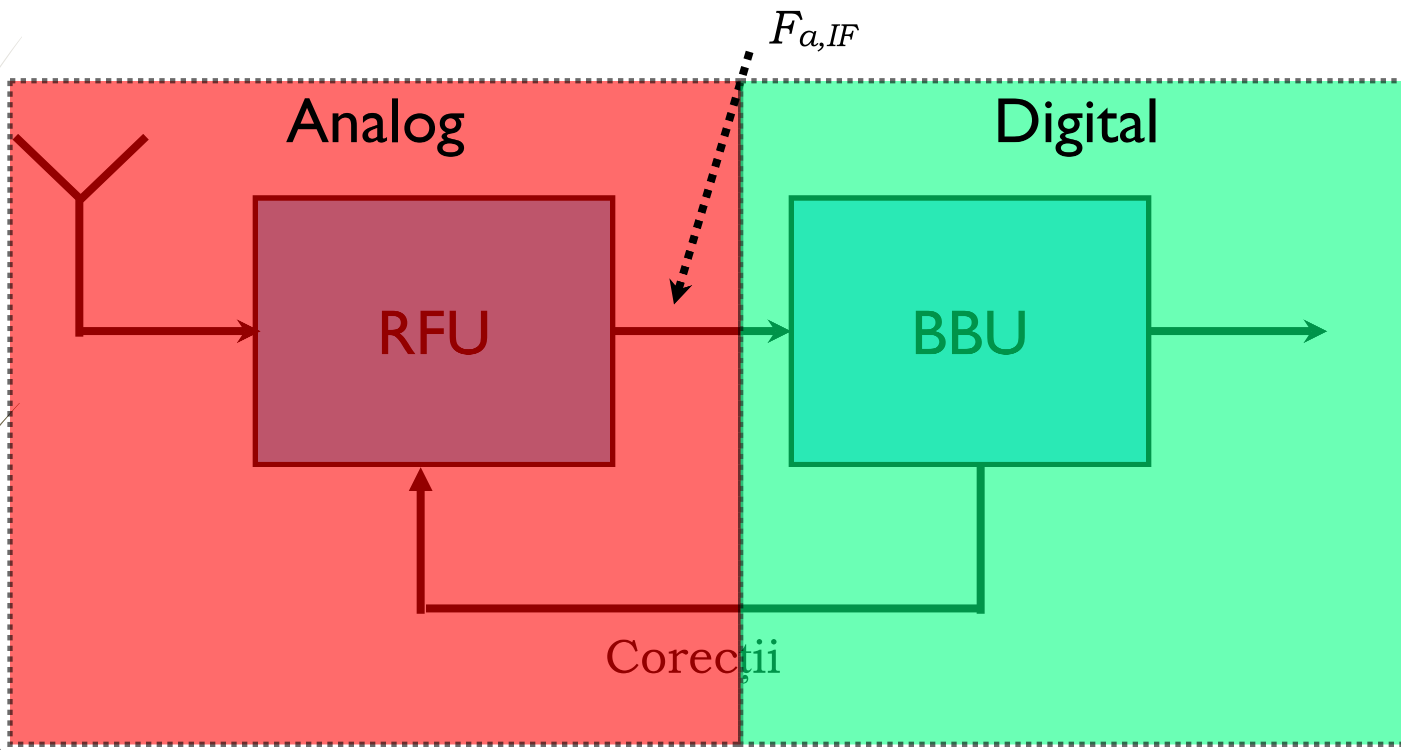
- Saturation:
  - Reference voltage: V_{REF}
  - Input resistance: R_{ADC}
  - Maximum admitted input power at the ADC input:

$$P_{ADC} = \frac{V_{REF}^2}{R_{ADC}}$$

Rx Architectures

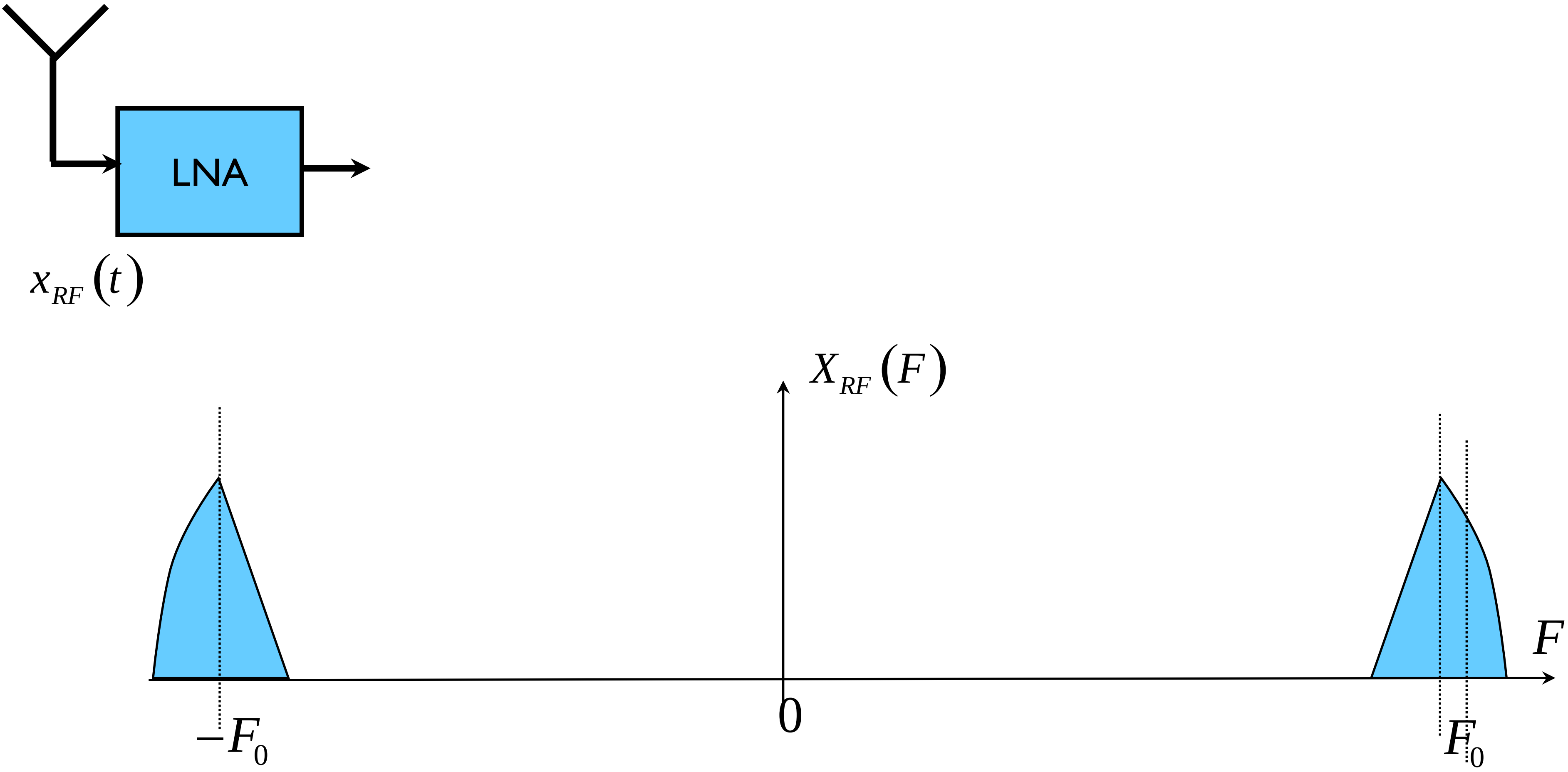
- The RR has an analog section and a digital section
  - A/D conversion
- Functions of the analog section
  - Amplification
  - Pre-filtering
  - Mixing from RF to IF or BB
- Functions of the digital section
  - Mixing to BB (optional)
  - Corrections (closed-loop or open-loop)
    - Carrier frequency
    - Amplification

Rx Architectures (2)

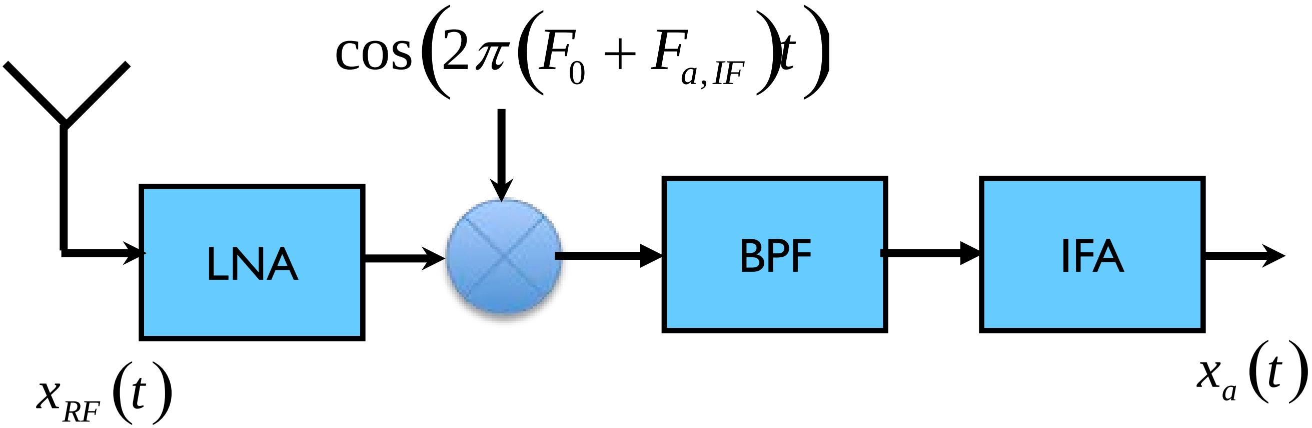


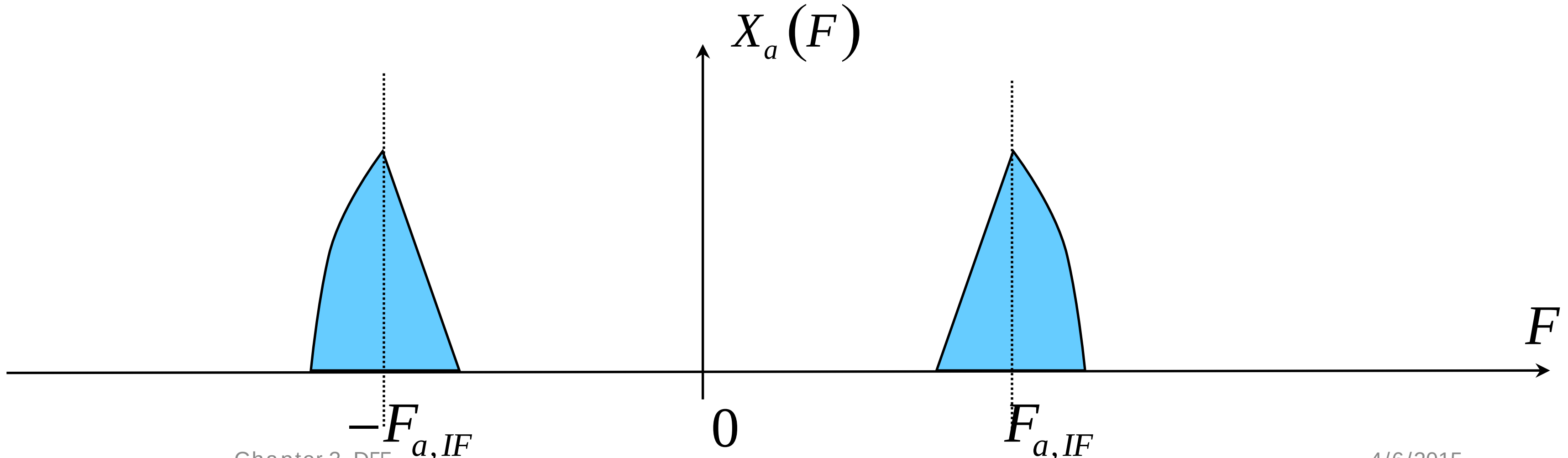
- $F_{a,IF}$
  - Zero: **Zero IF architecture**
  - Different form zero: **Digital IF architecture**
    - Requires digital mixing to BB (Digital Down Conversion - DDC)

Digital IF Architecture

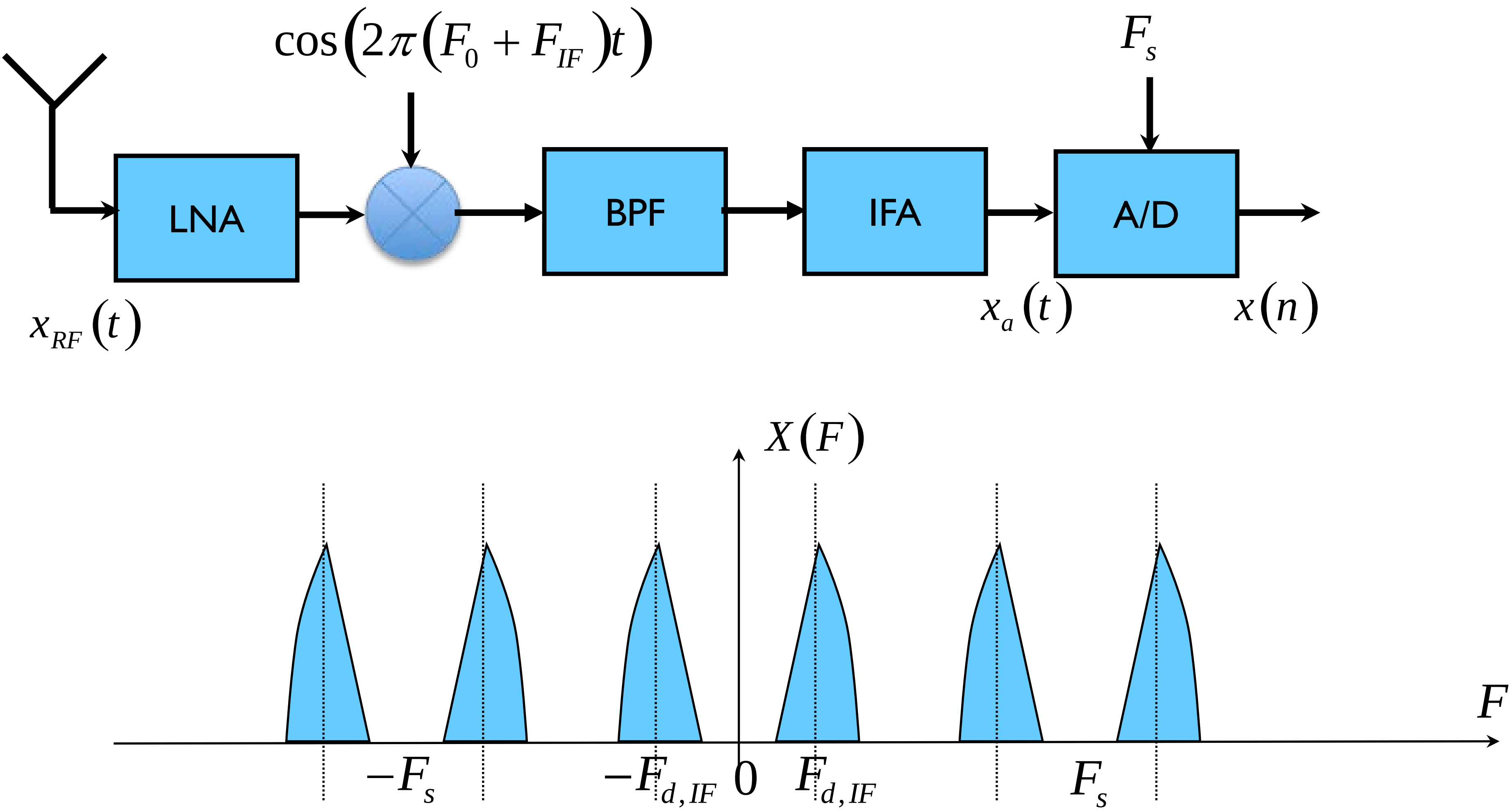


Digital IF Architecture (2)

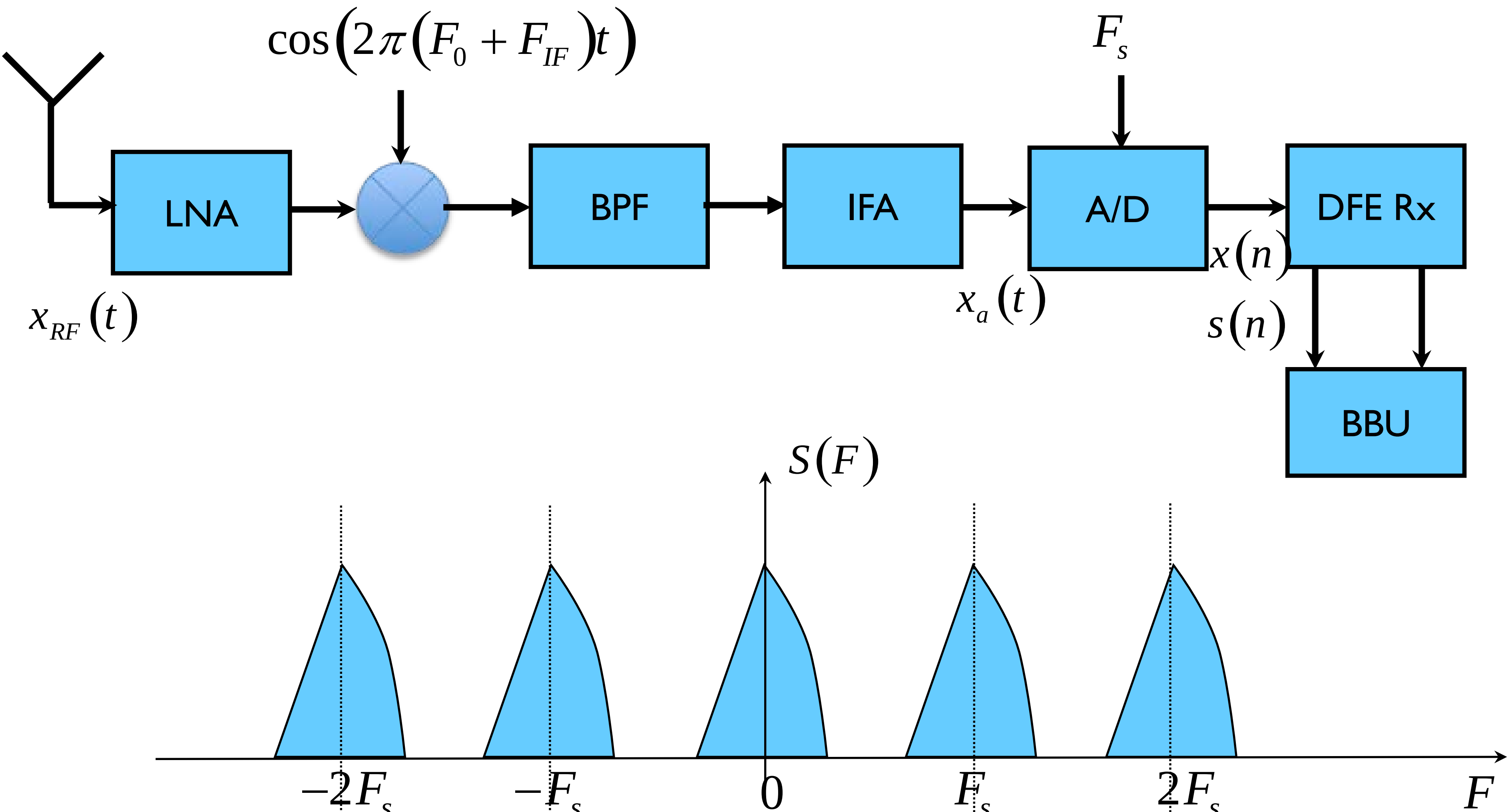




Digital IF Architecture (3)



Digital IF Architecture (4)

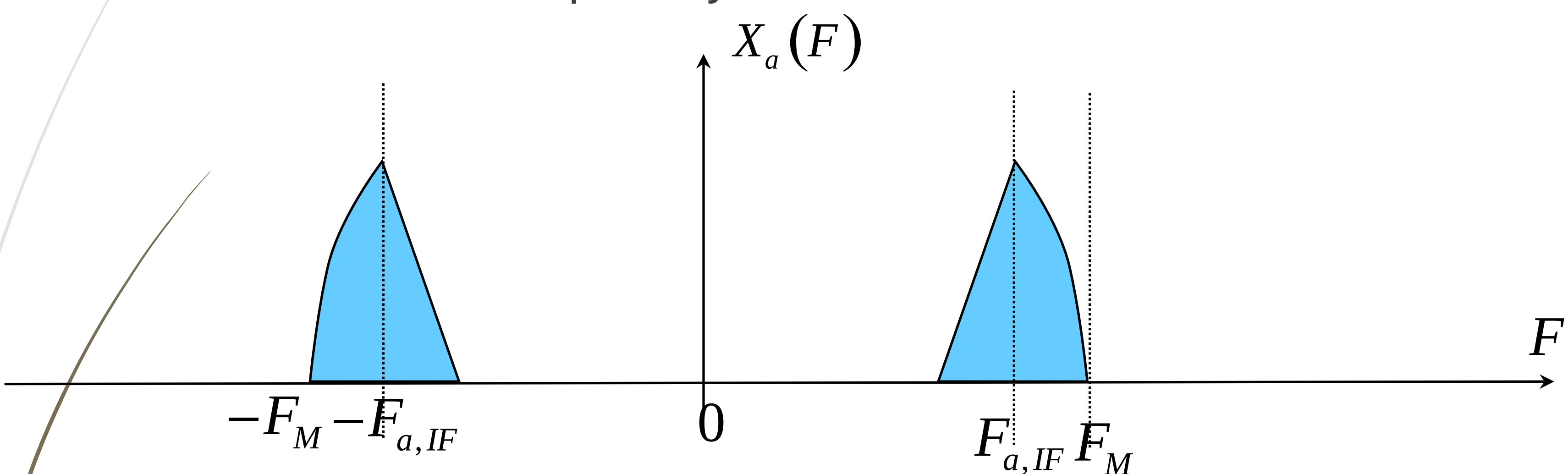


Signal sampling

- In the previously described diagram, two different intermediate frequencies are involved
  - In the analog domain: $F_{a,IF}$
  - In the digital domain: $F_{d,IF}$
- The spectrum of the signal is centered on $F_{a,IF}$ before the A/D conversion
- After the sampling operation, it is possible that the spectrum is centered on $F_{a,IF}$
  - If subsampling is used

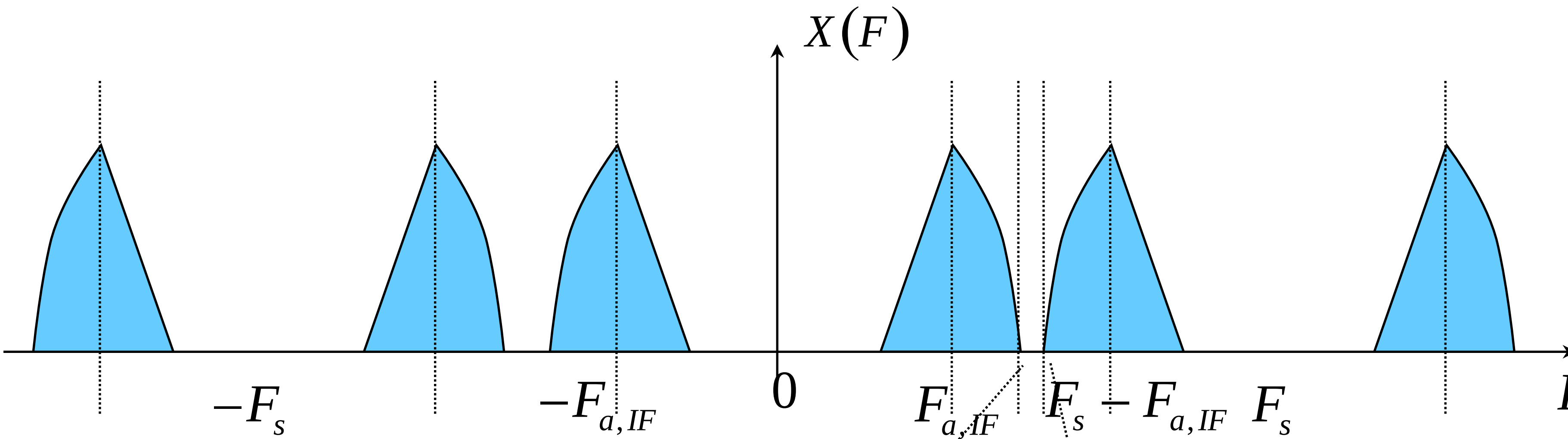
Signal sampling - example

- Signal bandwidth: 4 MHz
- Intermediate frequency: 70 MHz



- Maximum frequency: $F_M = 72MHz$
- According to Nyquist: $F_S > 2F_M = 144MHz$
  - A high frequency ADC is needed

Signal sampling – example (2)



$$F_{a,IF} + \frac{B}{2} \qquad F_s - F_{a,IF} - \frac{B}{2}$$

$$B_t = F_s - 2F_{a,IF} - B$$

$$b_t = \frac{B_t}{F_s} = 1 - \frac{2F_{a,IF} + B}{F_s}$$

$$b_t \gg \Rightarrow F_s \gg 2F_M$$

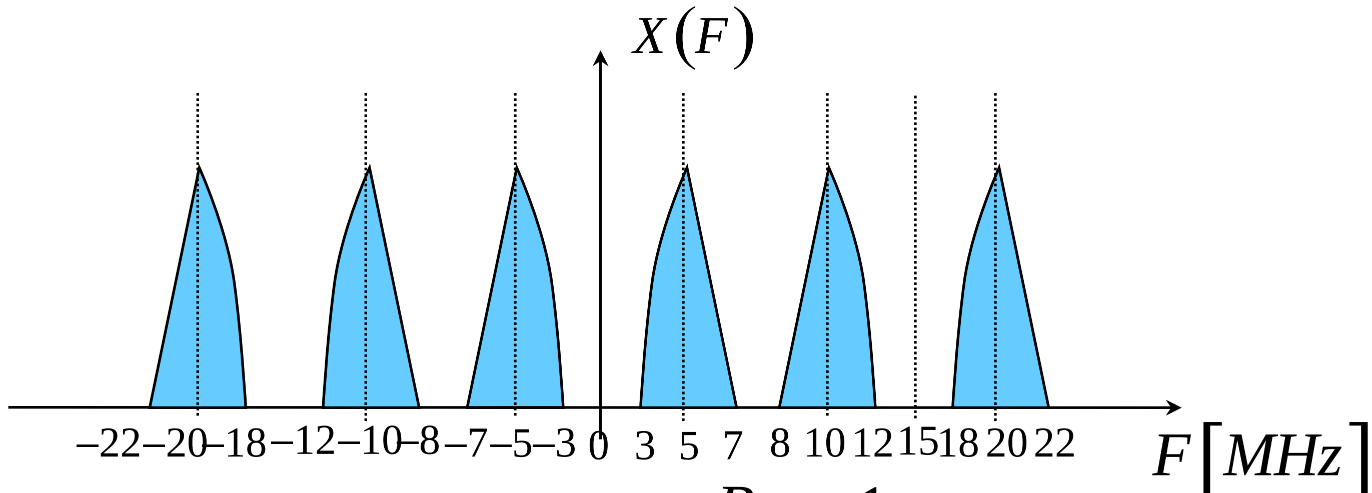
Signal sampling – example (3)

- Numerical example: F_S=200MHz
  - B_t=56MHz, b_t=0.28
- Sampling according to Nyquist
  - A high speed ADC is needed
  - In order to separate the usful spectrum from the image one, a highly complex digital filter is needed
- Alternative solution
  - **Subsampling**
  - The Nyquist theorem doesn't have to be literally complied with
    - The sampling frequency can be correlated not with the maximum frequency of the spectrum, but with the useful band of the signal, *B*
    - In reality, $F_s > 2B$

Signal subsampling

- If we sample the signal with F_S=15MHz
  - *15MHz << 200MHz*
- The spectrum from 70 MHz will also be found on $70 \pm 15k[MHz]$
  - 55, 40, 25, 10, -5, -20, -35, -50, -65, … [MHz]
- The spectrum from -70 MHz will also be found on $-70 \pm 15k[MHz]$
  - -55, -40, -25, -10, 5, 20, 35, 50, 65, … [MHz]

Signal subsampling (2)



$$B_t = 1MHz \qquad b_t = \frac{B_t}{F_S} = \frac{1}{15}$$

$$F_{d,IF} = 5MHz \neq F_{a,IF} = 70MHz$$

- The ADC works on a much lower frequency, so it is much cheaper
- The spectrum is reversed in this case

Subsampling – general case

- If we sample the signal with F_S
- The spectrum on $F_{a,IF}$ *will be found also on* $F_{a,IF} \pm kF_S$
- The spectrum on $-F_{a,IF}$ *will be found also on* $-F_{a,IF} \pm kF_S$
- The spectrum can be found on
  - $\langle F_{a,IF} \rangle_{F_s}$, coming from the image from $F_{a,IF}$
  - $\langle -F_{a,IF} \rangle_{F_s}$, coming from the image from $-F_{a,IF}$

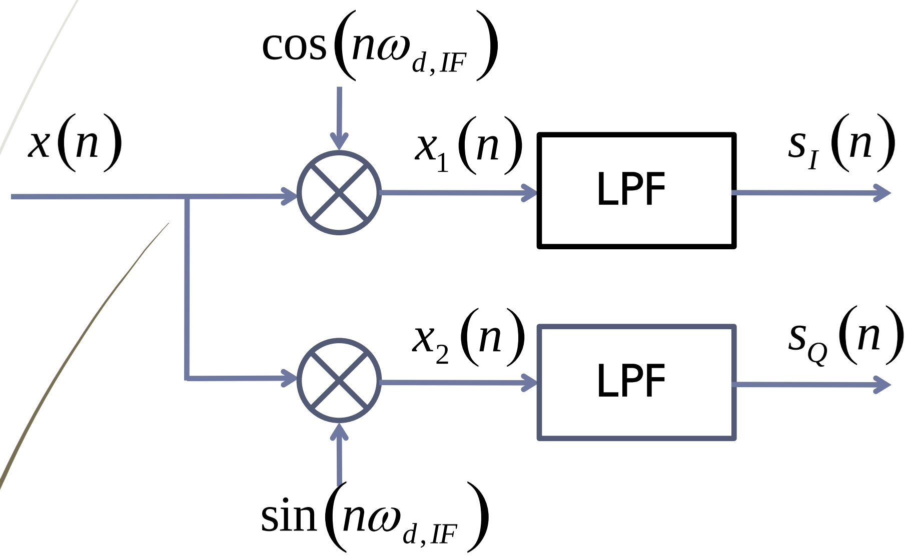
$$F_{d,IF} = \min \left\{ \langle F_{a,IF} \rangle_{F_s}, \langle -F_{a,IF} \rangle_{F_s} \right\}$$

Subsampling – general case (2)

Region	$F_{a,IF}$	Reversed spectrum?	Mixing frequency
1	$0 \ldots F_s/2$	No	0
2	$F_s/2 \ldots F_s$	Yes	$F_s - F_{a,IF}$
3	$F_s \ldots 3F_s/2$	No	$F_{a,IF} - F_s$
4	$3F_s/2 \ldots 2F_s$	Yes	$2F_s - F_{a,IF}$
5	$2F_s \ldots 3F_s/2$	No	$F_{a,IF} - 2F_s$
6	$5F_s/2 \ldots 3F_s$	Yes	$3F_s - F_{a,IF}$
7	$3F_s \ldots 7F_s/2$	No	$F_{a,IF} - 3F_s$
8	$7F_s/2 \ldots 4F_s$	Yes	$4F_s - F_{a,IF}$

Quadrature demodulation

$$x(n) = s_I(n)\cos(n\omega_{d,IF}) - s_Q(n)\sin(n\omega_{d,IF}) \qquad \omega_{d,IF} = 2\pi \frac{F_{d,IF}}{F_s}$$



$$x_1(n) = \frac{1}{2}s_I(n) + \frac{1}{2}s_I(n)\cos(2n\omega_{d,IF}) - \frac{1}{2}s_Q(n)\sin(2n\omega_{d,IF})$$

$$x_2(n) = -\frac{1}{2}s_Q(n) + \frac{1}{2}s_I(n)\sin(2n\omega_{d,IF}) + \frac{1}{2}s_Q(n)\cos(2n\omega_{d,IF})$$

Quadrature demodulation (2)

- Similar to the transmitter case
  - The multiplication is simpler if

$$F_{d,IF} = \frac{F_S}{4} \qquad F_{d,IF} = \frac{F_S}{8}$$

- It is useful for the sampling to be performed in such a way that one of the above relations are obtained
- Example:

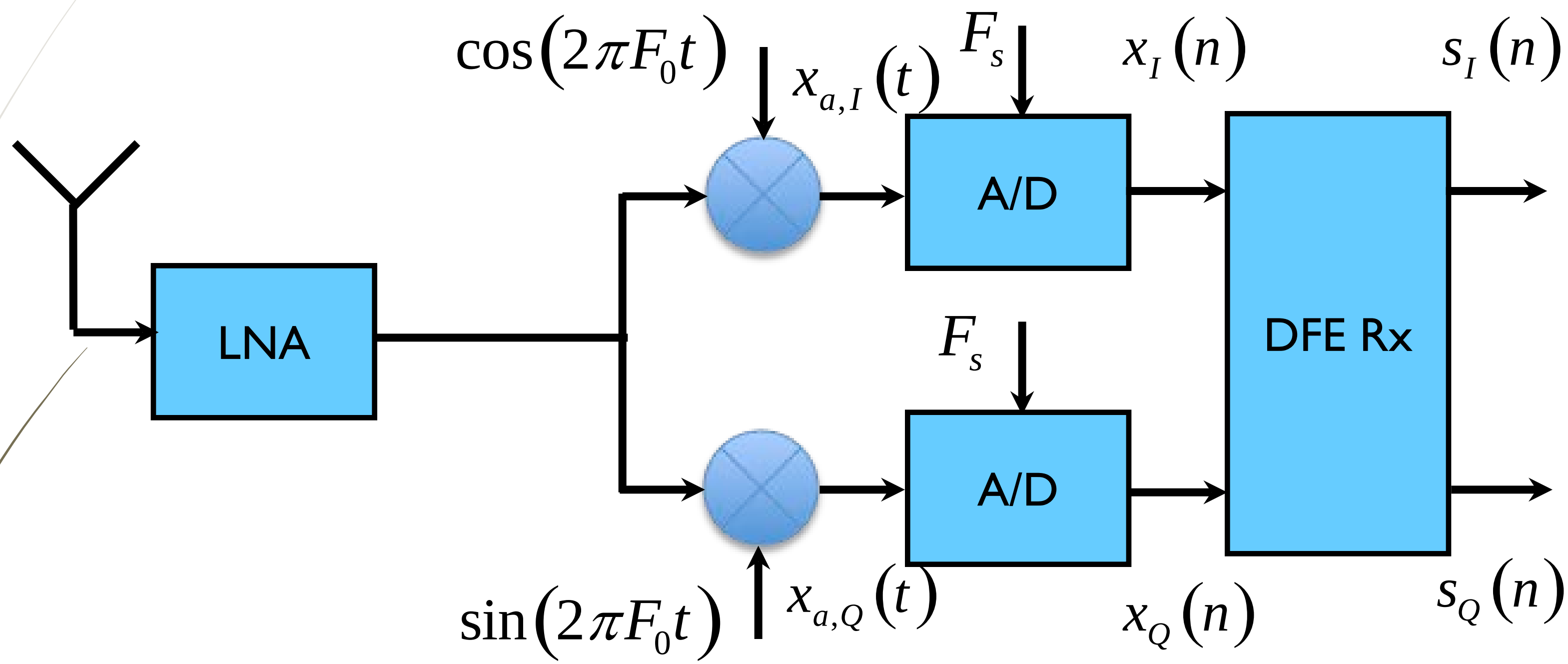
$$\left\langle F_{a,IF} \right\rangle_{F_s} = \frac{F_s}{4} \Rightarrow F_{a,IF} - kF_s = \frac{F_s}{4} \qquad F_{a,IF} = \left(k + \frac{1}{4}\right) F_s$$

- If $F_{a,IF}$=70MHz, F_S=56MHz => $F_{d,IF}$=14MHz

Zero IF Architecture

- The intermediate IF architecture is based on the superheterodyne principle of the analog receivers
  - Problems with:
    - The high complexity
    - The image spectra: $F_0+2F_{a,IF}$
- Alternative:
  - The synchrodyne receiver (direct-conversion receiver, zero-IF receiver, homodyne receiver)
  - Converts directly to baseband

Zero IF Architecture (2)

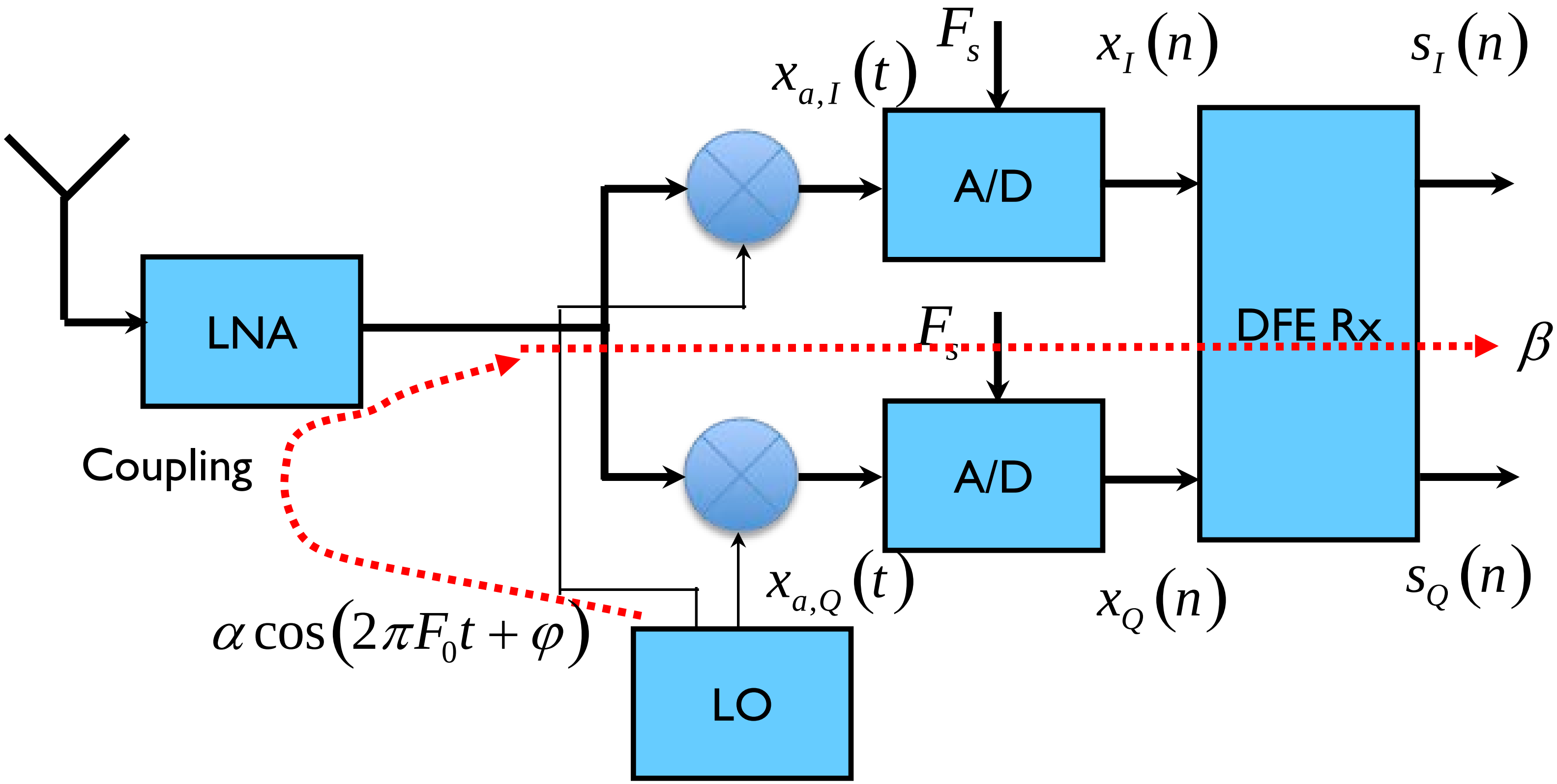


- The analog oscillator is a quadrature one
- Two A/D converters are needed

Zero IF Problems

- Parasite DC component
  - Leakage of the signal from the local oscillator
  - Receiver penetration by a perturbation signal
- Phase noise
- Oscillator imbalance
- 2nd order distortions
- Retransmission of the local oscillator signal

Parasite DC component



Parasite DC component (2)

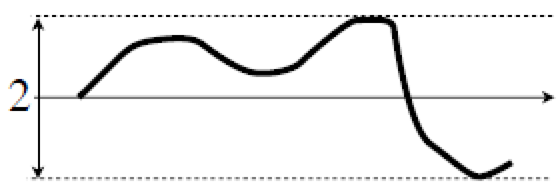
- The presence of a DC component reduces the allowed dynamic range
  - In the digital part: |Signal Amplitude|≤1
    - The signal is composed of the useful signal and the DC component

$$|\beta + s(n)| \leq 1$$

    - If β>0

$$|s(n)|_{max} = 1 - \beta$$

- Limitation of the dynamic range and of the peak power

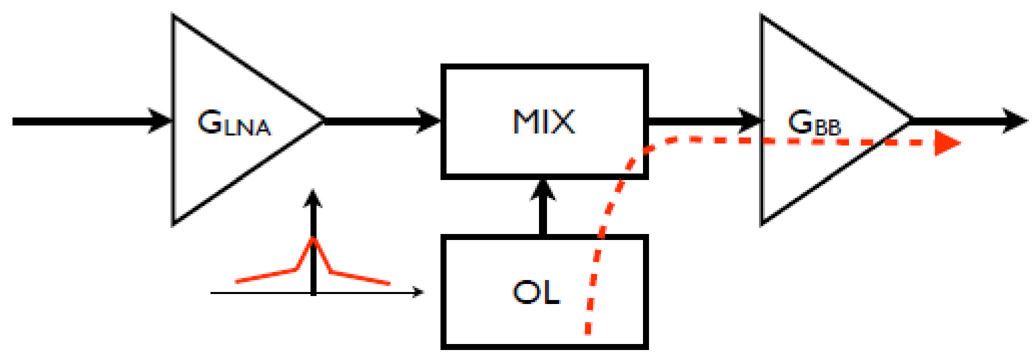


No DC component

With DC Component

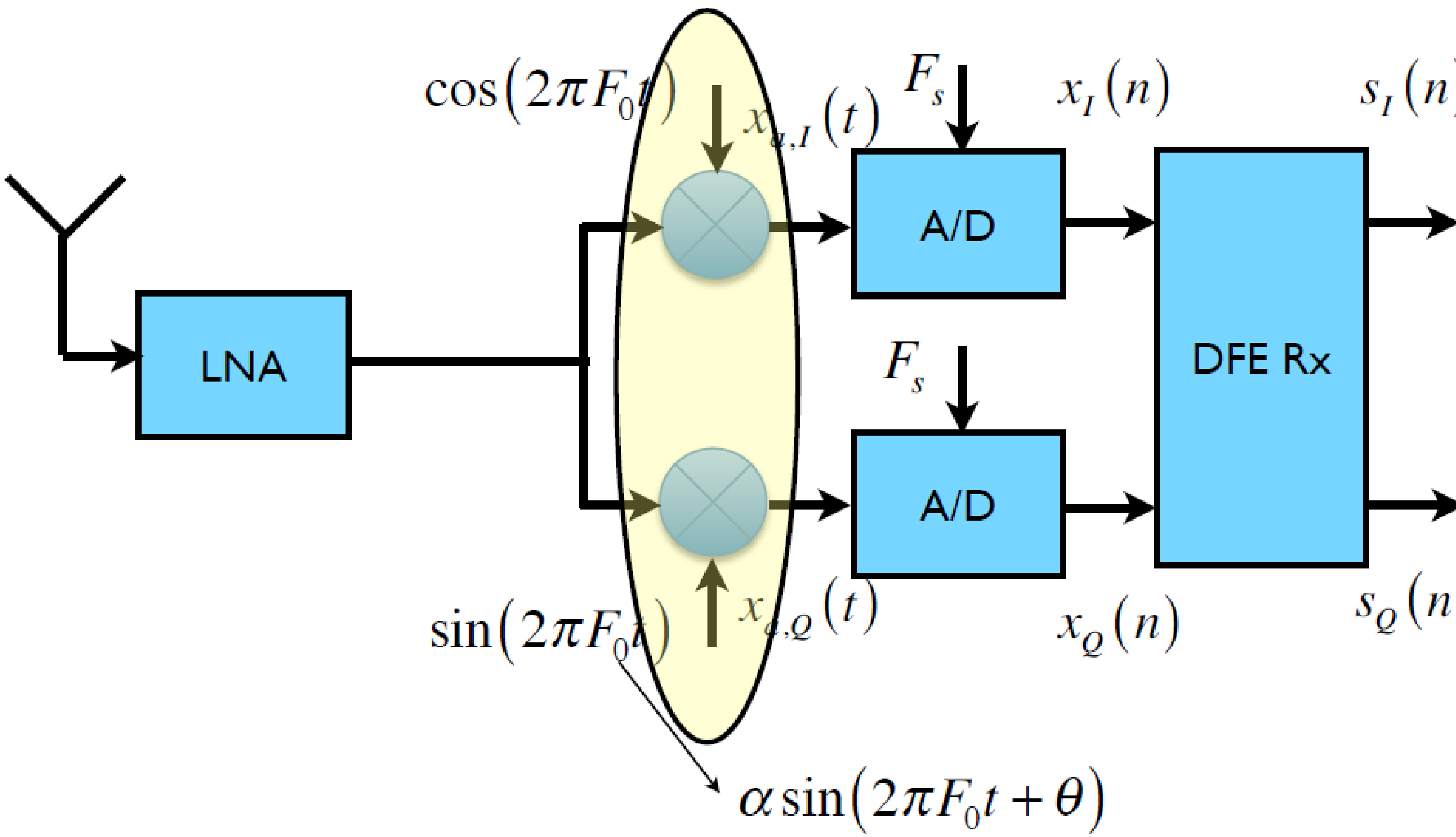
Phase noise for ZIF receiver

- Small number of stages
  - A large amount of amplification will be performed in baseband
  - The simplified diagram of the amplification chain:

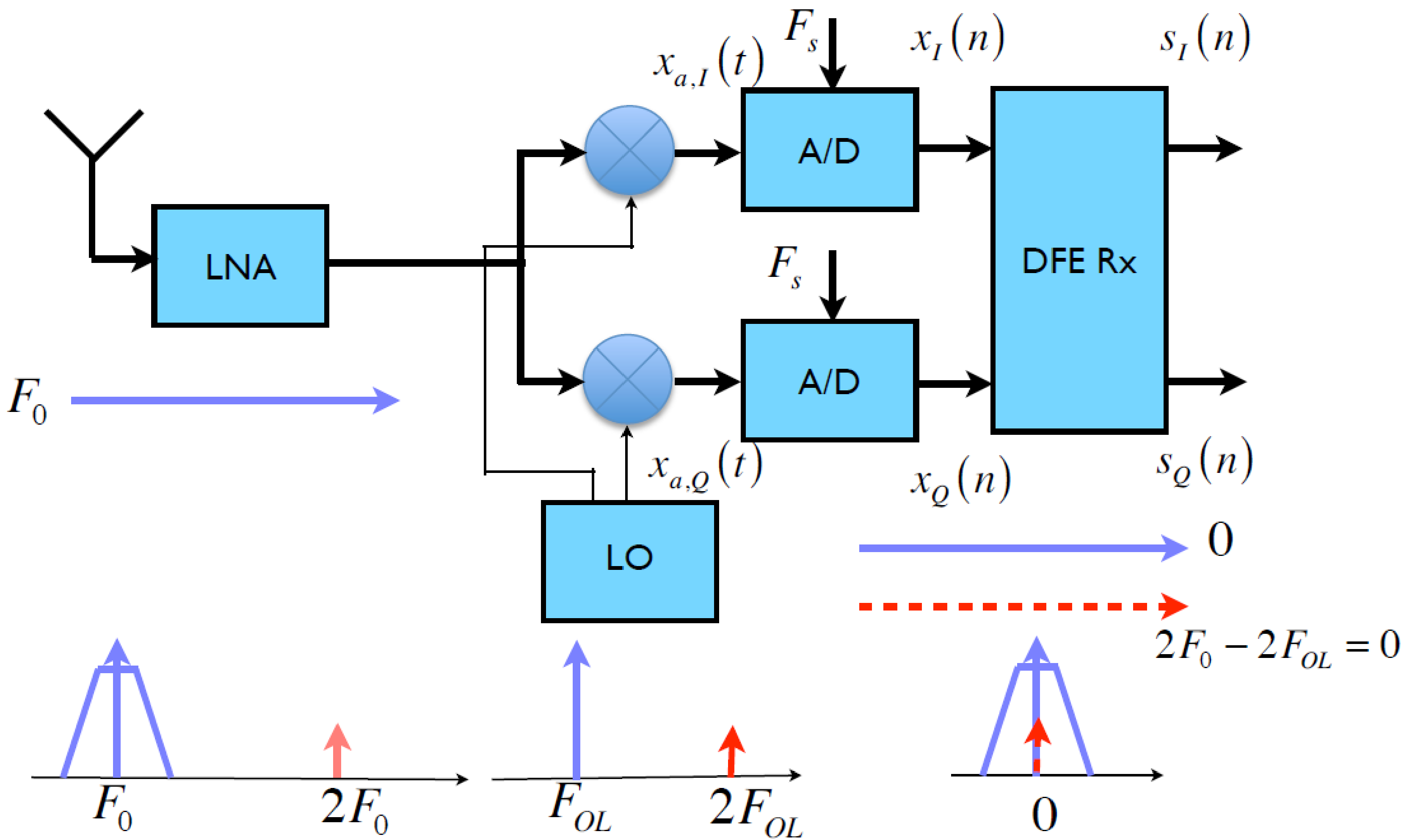


- The noise produced by the LO can be strongly amplified in baseband
  - Important problems with the phase noise (important: Flicker noise – 1/f)

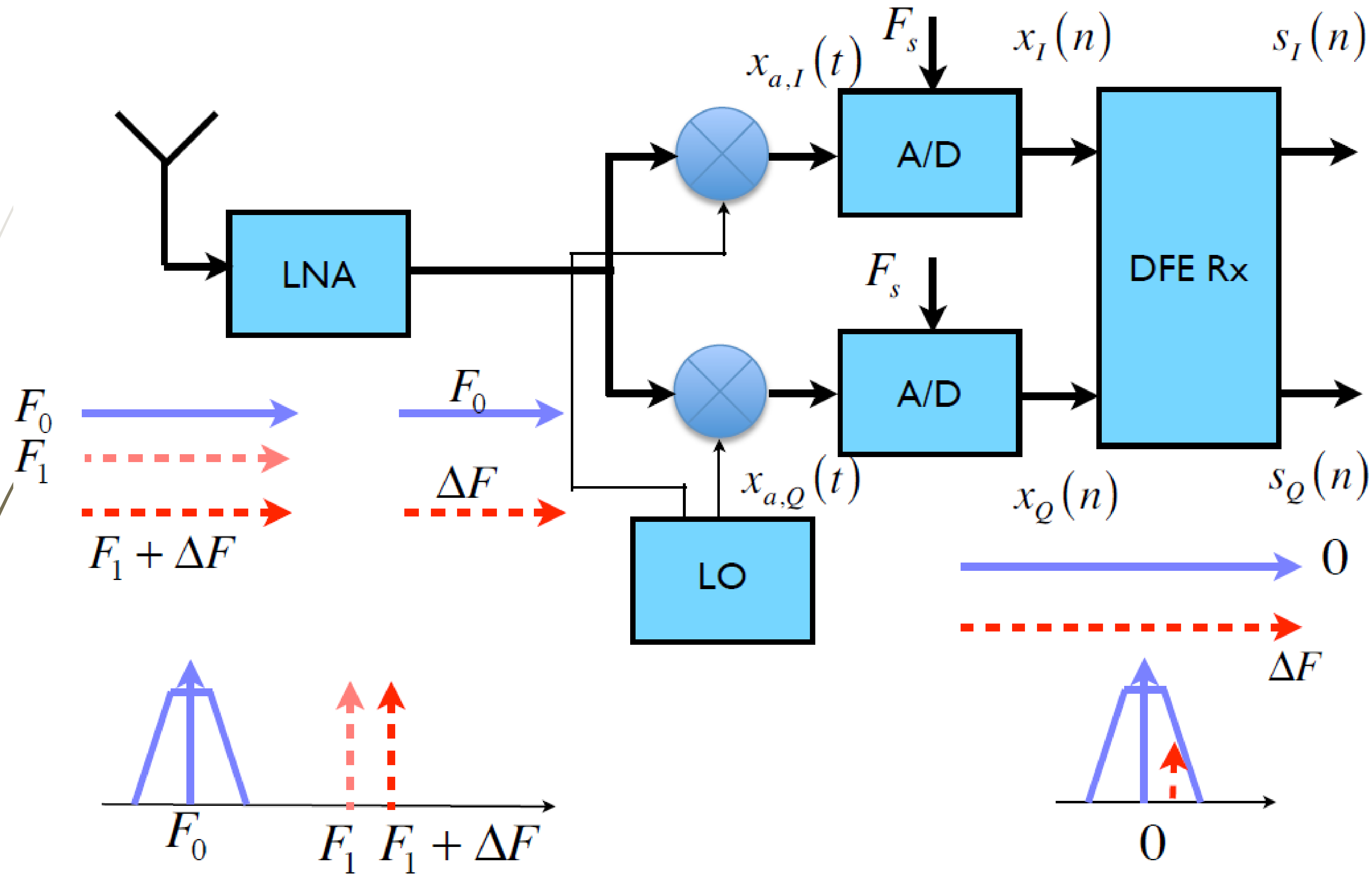
Oscillator imbalance



2nd order distortions



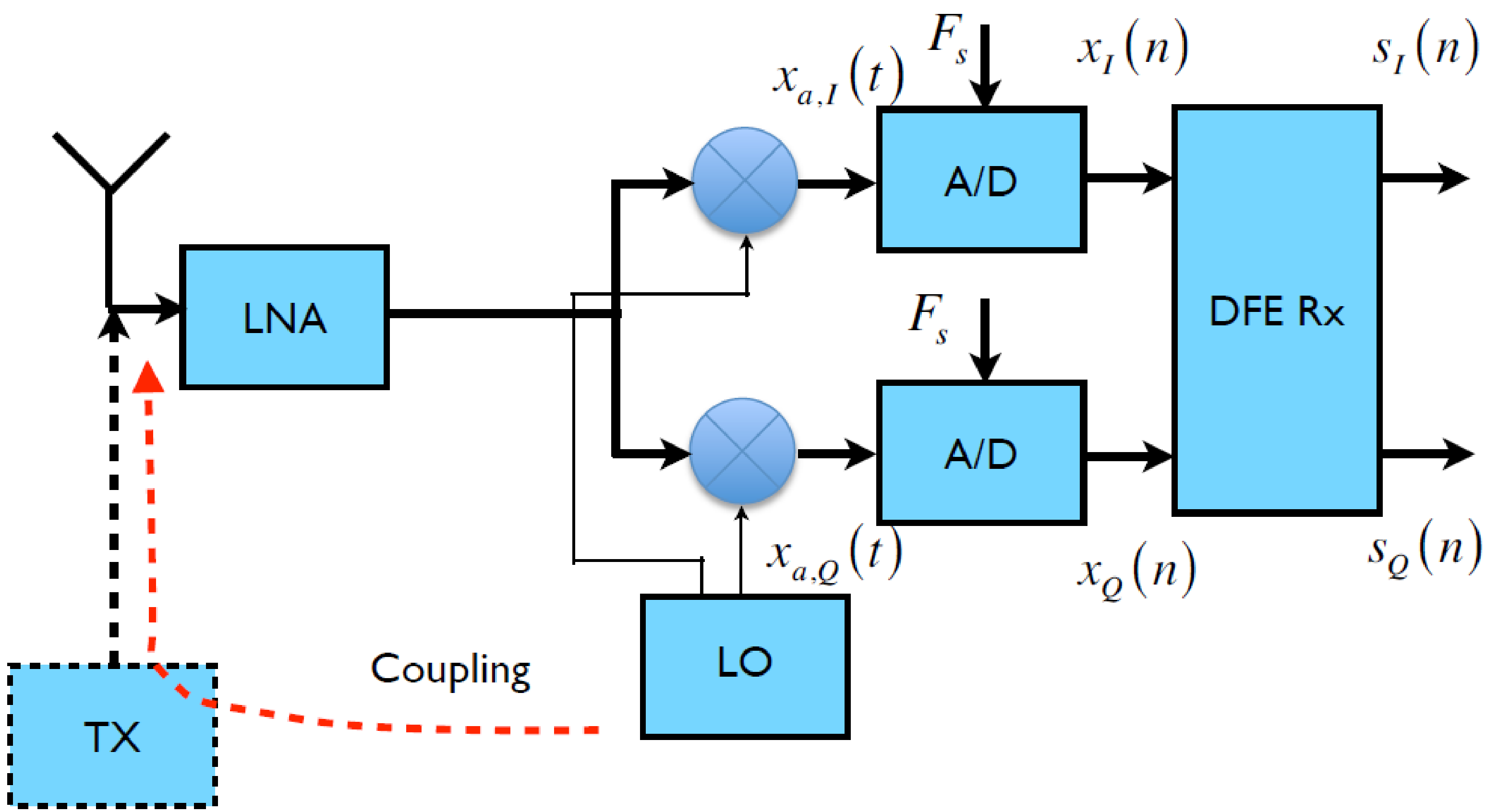
2nd order distortions (2)



2^{nd} order distortions (3)

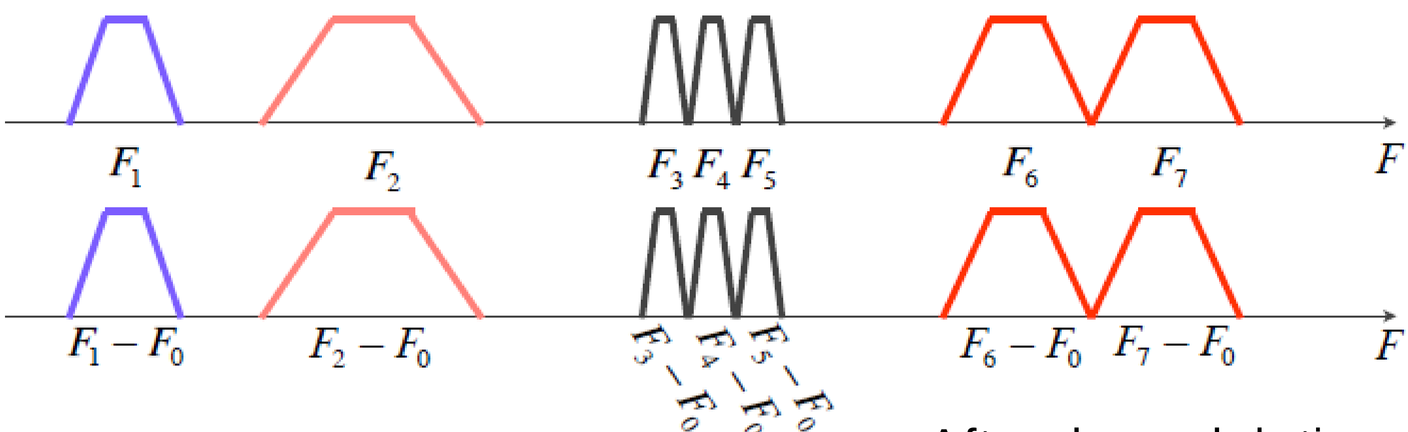
- In the ZIF receivers the 2^{nd} order distortions are the ones that count
  - As a general rule, the even ones
  - IIP2
- The obtained effect is the presence of a parasite DC component in baseband
- For the superheterodyne receiver the 3^{rd} order distortions are the ones that count
  - IIP3

Retransmission of the LO signal



Multiband architectures

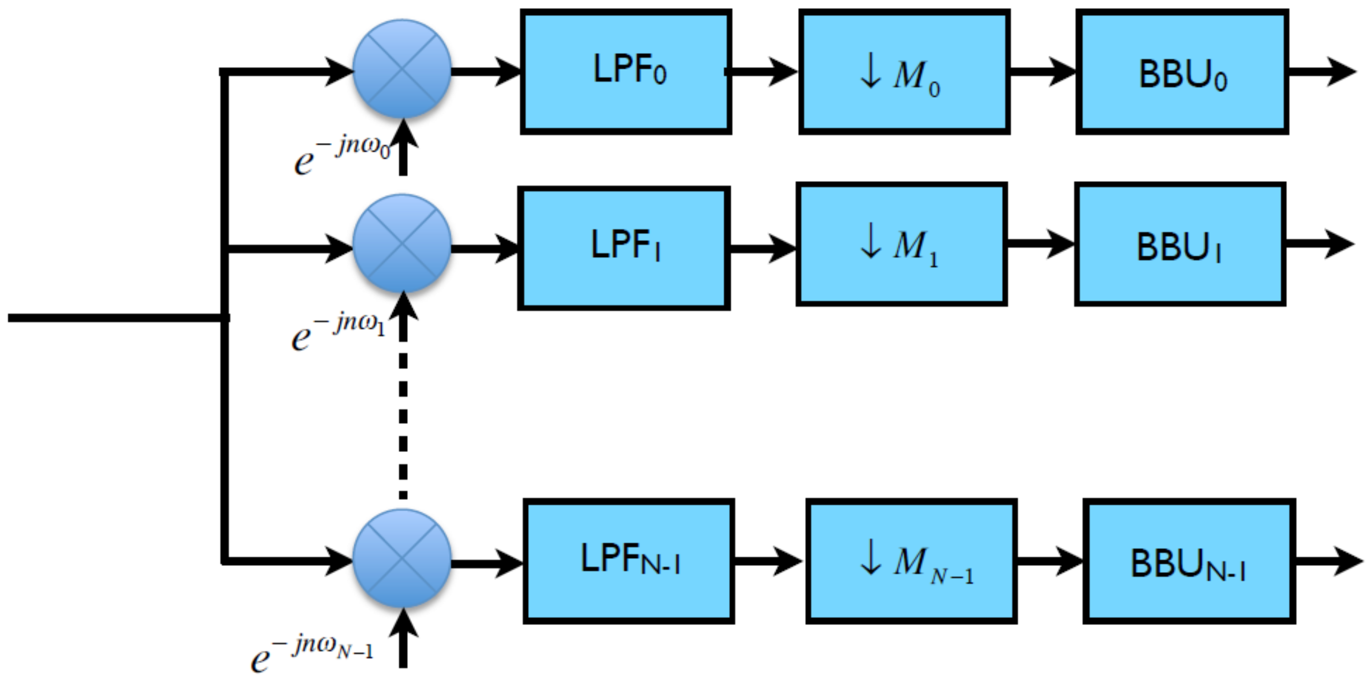
- Possible using ZIF receivers
- The signal is composed from several spectra, of different bandwidths, centered on different frequencies (SDR principle)
- Different communication standards



After demodulation

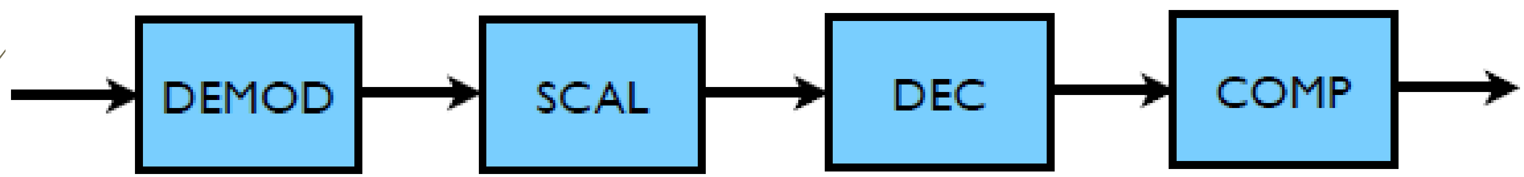
Multiband architectures (2)

- Channel separation is performed in DFE Rx
  - A wideband analog section is necessary (including antenna)



DFE Rx Signal Processing Chain

- Some blocks can be missing
- The order is not compulsory
- The processing of a single channel is considered



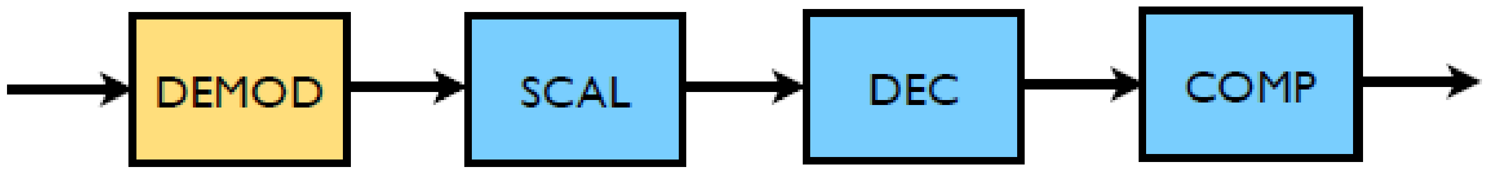
DEMOD – performs signal mixing towards baseband

SCAL – scales the signal for an optimal processing

DEC – converts the sampling frequency, in order to use a minimum rate, adapted to the channel bandwidth

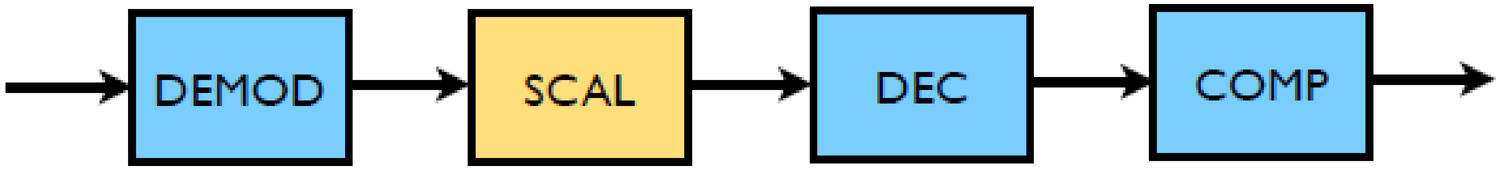
COMP – estimates and corrects some receiver parameters

Signal demodulation



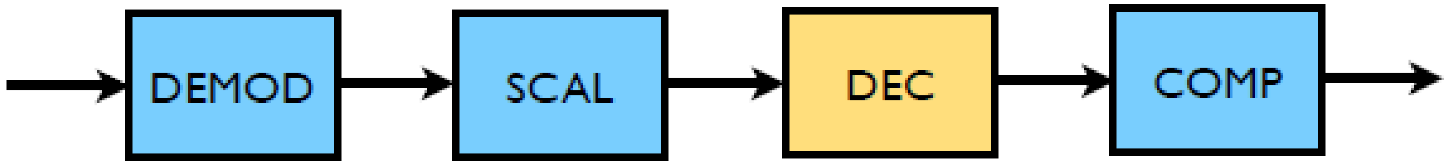
- The block is used only in case of the digital IF architecture
- The complexity of the block is similar to the MOD block from DFE Tx

Level scaling



- The power level is adjusted for an optimal processing in the baseband section
- Same principle as for Tx

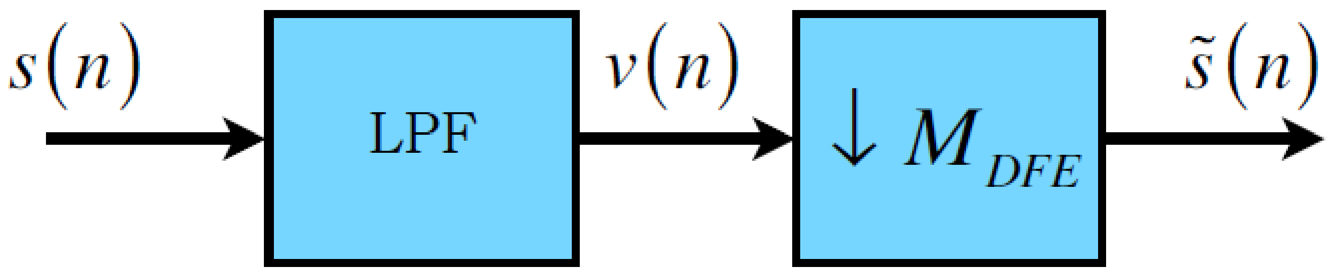
Signal decimation



- The signal spectrum before the A/D converter is not perfectly limited to the occupied band
  - The analog filtering cannot limit the bandwidth, using a medium complexity
- The signal is oversampled
  - If the sampling theorem is considered as $F_S>2F_M$, then we talk about subsampling
  - If the band-pass signal sampling theorem is used and $F_S>2B$, then a oversampling is used
- A decimation is necessary

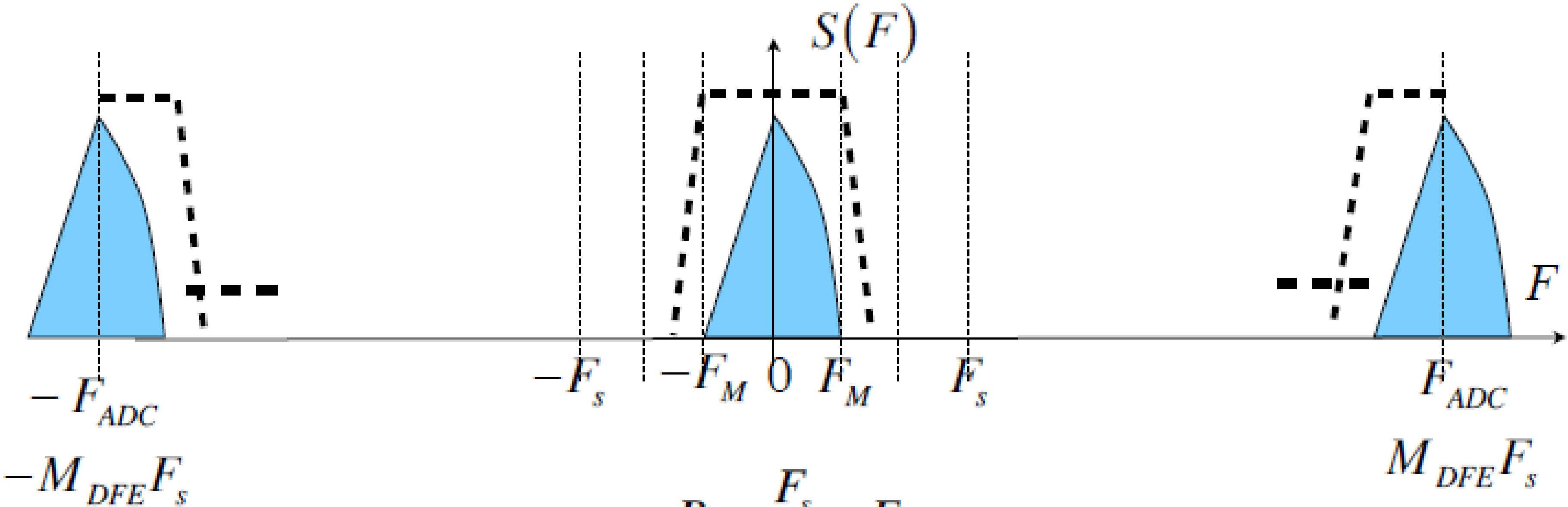
Decimation filter

- The decimation filter is made of:
  - A complex low-pass filter (2 real filters for I+Q)
  - An elementary decimator



- **Goal:** limit the signal spectrum
  - After the decimator, aliasing has to be avoided
  - The Nyquist condition has to be observed after the decimation

Decimation filter (2)



$$B_t = \frac{F_s}{2} - F_M$$

$$b_t = \frac{B_t}{F_{ADC}} = \frac{B_t}{M_{DFE}F_s} = \frac{\frac{F_s}{2} - F_M}{M_{DFE}F_s} = \frac{1}{2M_{DFE}} - \frac{F_M}{M_{DFE}F_s}$$

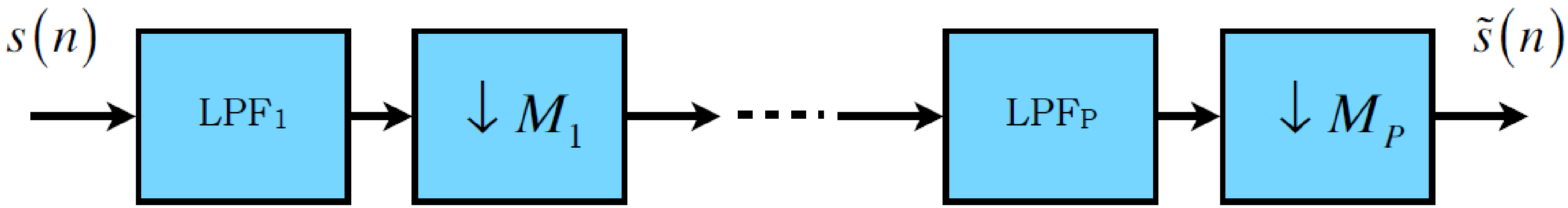
Decimation filter (3)

- Example:
  - F_M=0.75MHz
  - F_{ADC}=16MHz
  - M_{DFE}=8

$$b_t = \frac{1-0.75}{16} = \frac{1}{64}$$

- The resulted filter can be very complex
- The decimation has to be done in steps

Decimation chain



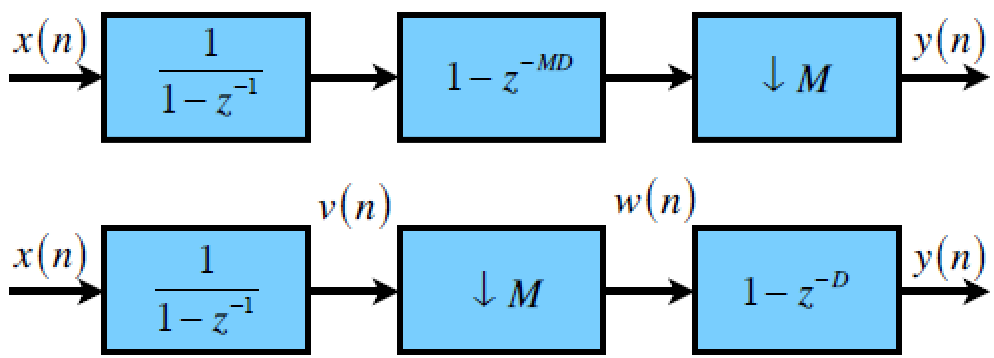
$$M_{DFE} = \prod_{p=1}^{P} M_p$$

- The complexity of the filters increases along the chain
- For the first stages, CIC filters can be used

CIC Filters

- Very fast decimation filters
- Ideal for FPGA implementation

$$H(z) = \frac{1 - z^{-MD}}{1 - z^{-1}}$$



Compensations

- Modules based on digital algorithms
- Compensate the imbalances produced by the analog circuits (DC, phase, aso.)
- The imbalances can be:
  - Estimated and compensated
    - The estimate is fed back to the analog section
    - Large deviations are estimated and compensated with higher errors
    - A reaction path is necessary (D/A conversion)
  - Only compensated
    - No feedback to the analog domain

Compensations (2)

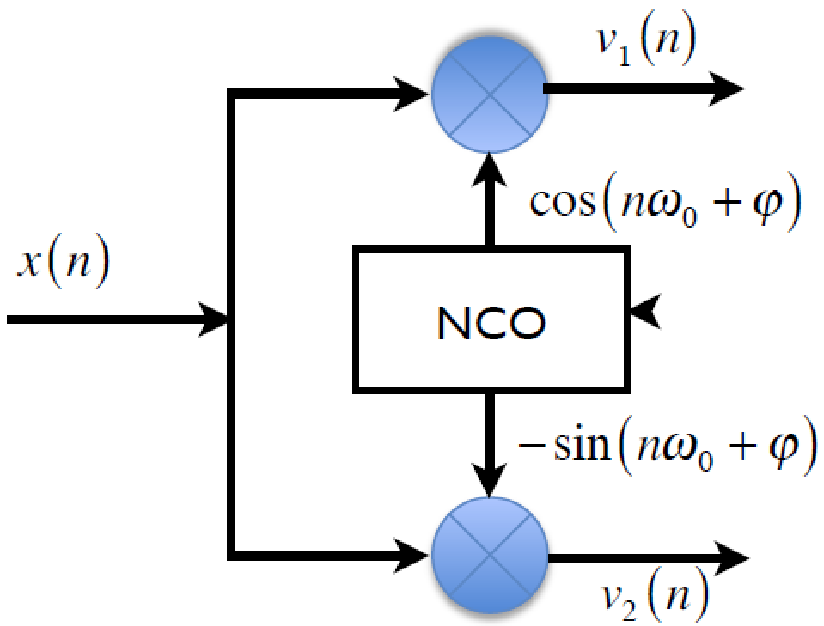
- DC Offset Compensation
  - Compensation: High-Pass Filtering
  - Estimation: measurement during a silent period
- Automatic Gain Control (AGC)
  - Goal: maximize the dynamic range of the signal
  - 2 solutions which are not exclusive:
    - Analog AGC (compensates the slow fading)
    - Digital AGC
      - Open-loop: the level is adjusted for further processing
      - Closed-loop: commands a programmable analog attenuator (optimal ADC attack)

Receiver synchronization

- Types:
  - Carrier synchronization
    - Frequency
    - Phase
  - Clock synchronization
  - Time synchronization
- Most of the algorithms are digital ones
  - Open-loop synchronization (only a digital correction)
  - Closed-loop synchronization (feedback to analog)

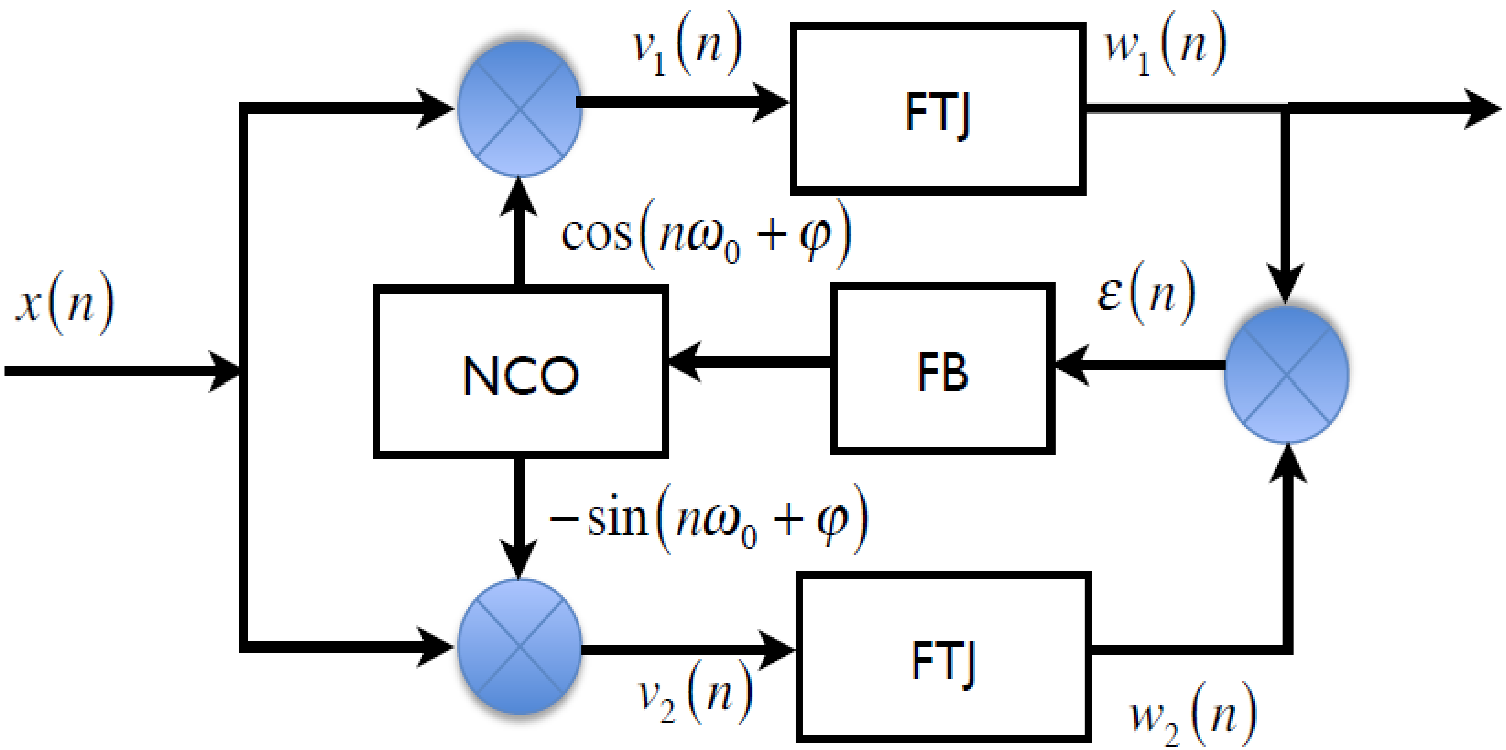
Carrier synchronization

- Example: **Costas Loop**
  - Alternative to non-linear schemes
  - Removes the modulating signal through linear transforms



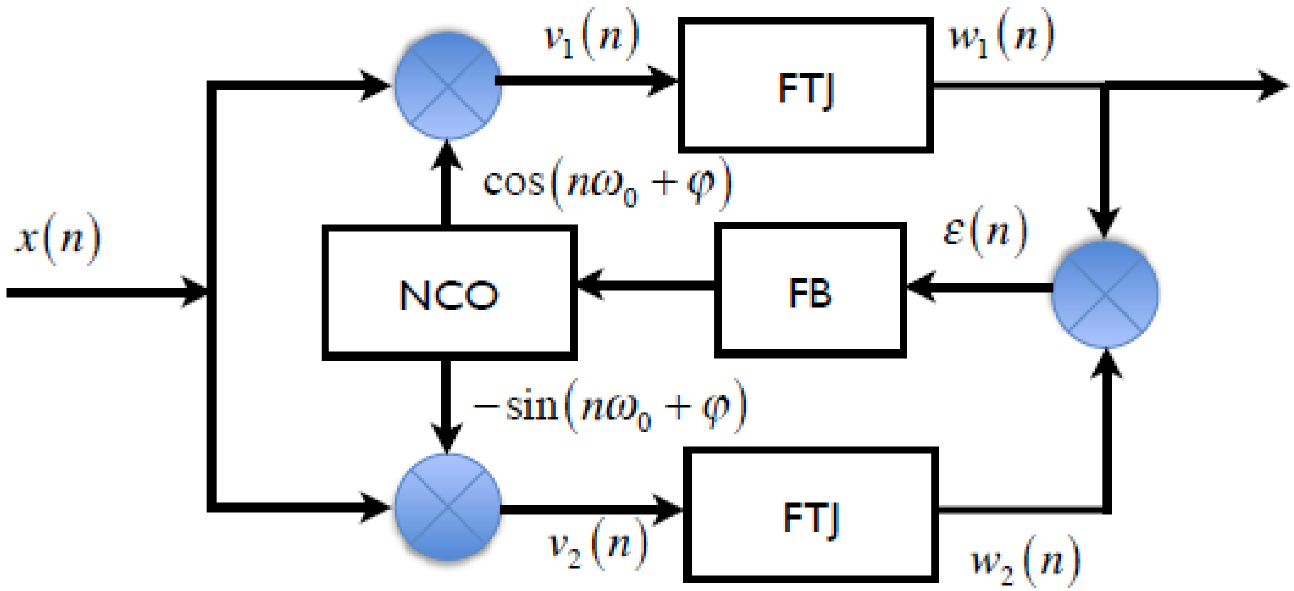
$$v_1(n)=\frac{1}{2}\cos\varphi+\frac{1}{2}\cos(2nw_0) \qquad v_2(n)=\frac{1}{2}\sin\varphi+\frac{1}{2}\sin(2nw_0)$$

Costas Loop (2)



$w_1(n) = \cos\varphi$ $\qquad$ $w_2(n) = \sin\varphi$

Costas Loop for BPSK signals

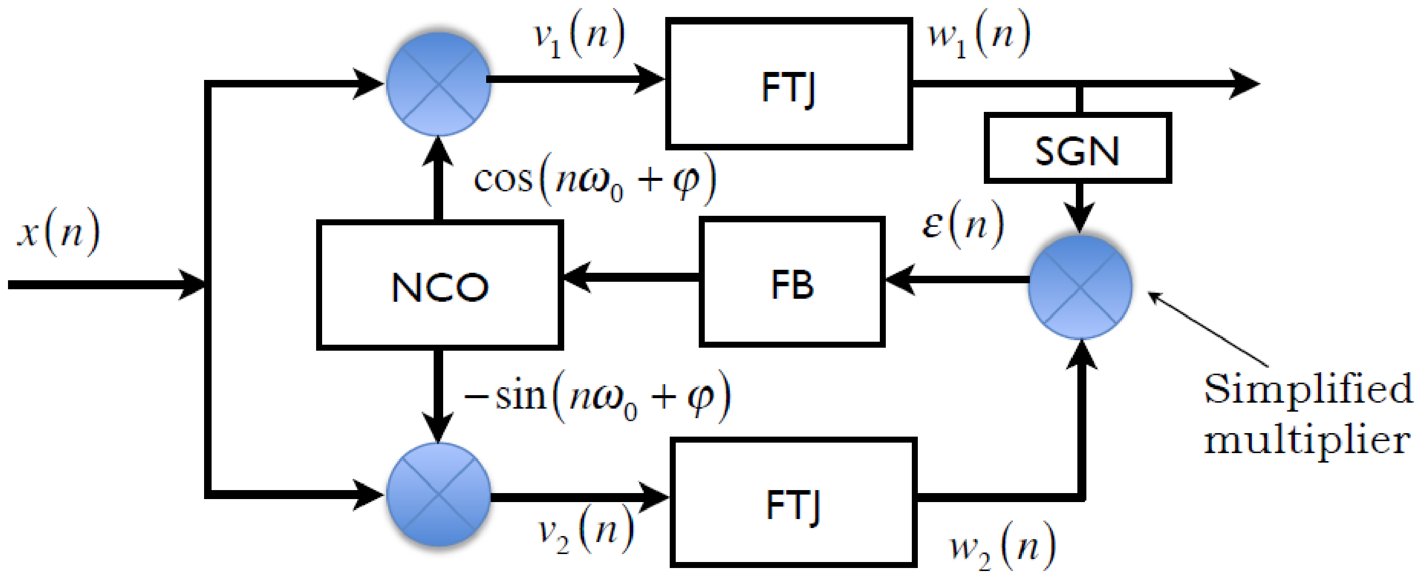


$$x(n) = d(n)\cos(n\omega_0) \qquad d(n) \in \{\pm 1\}$$

$$w_1(n) = \frac{1}{2}d(n)\cos\varphi \qquad w_2(n) = \frac{1}{2}d(n)\sin\varphi$$

$$\varepsilon(n) = d^2(n)\sin 2\varphi = \sin 2\varphi \approx 2\varphi$$

Costas Loop for BPSK signals (2)



$$x(n) = d(n)\cos(n\omega_0) \qquad d(n) \in \{\pm 1\}$$

$$w_1(n) = \frac{1}{2} d(n)\cos\varphi \qquad w_2(n) = \frac{1}{2} d(n)\sin\varphi$$

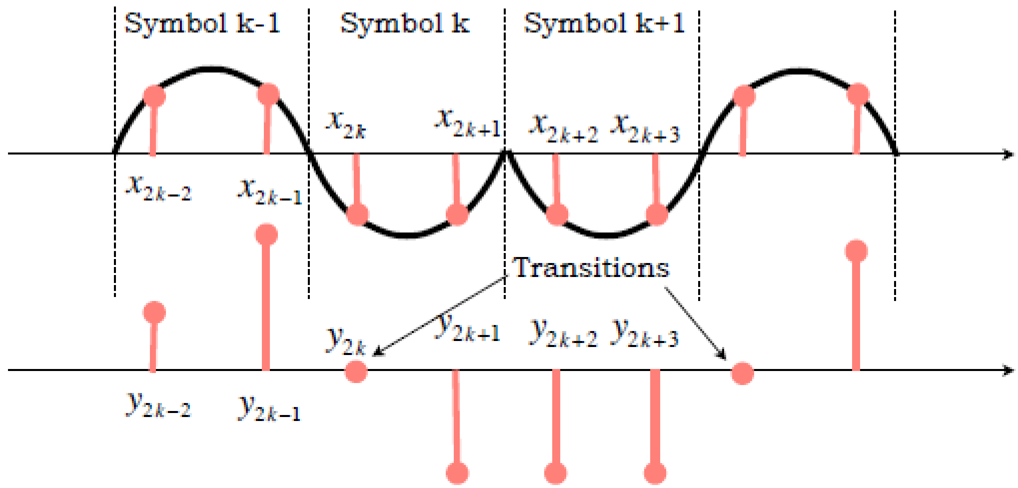
$$\varepsilon(n) = d(n)\,\mathrm{sgn}\{d(n)\}\sin 2\varphi = \sin 2\varphi \approx 2\varphi$$

Timing synchronization

- Necessary in order to detect the beginning of the symbol for the modulating signal
- Variants:
  - Detection of the transition between the symbols
    - Based on a uniformity of the bit distribution
  - Detection of the middle of the symbol
  - Preamble detection
    - Known sequence, both at transmission and at reception

Half-symbol integration

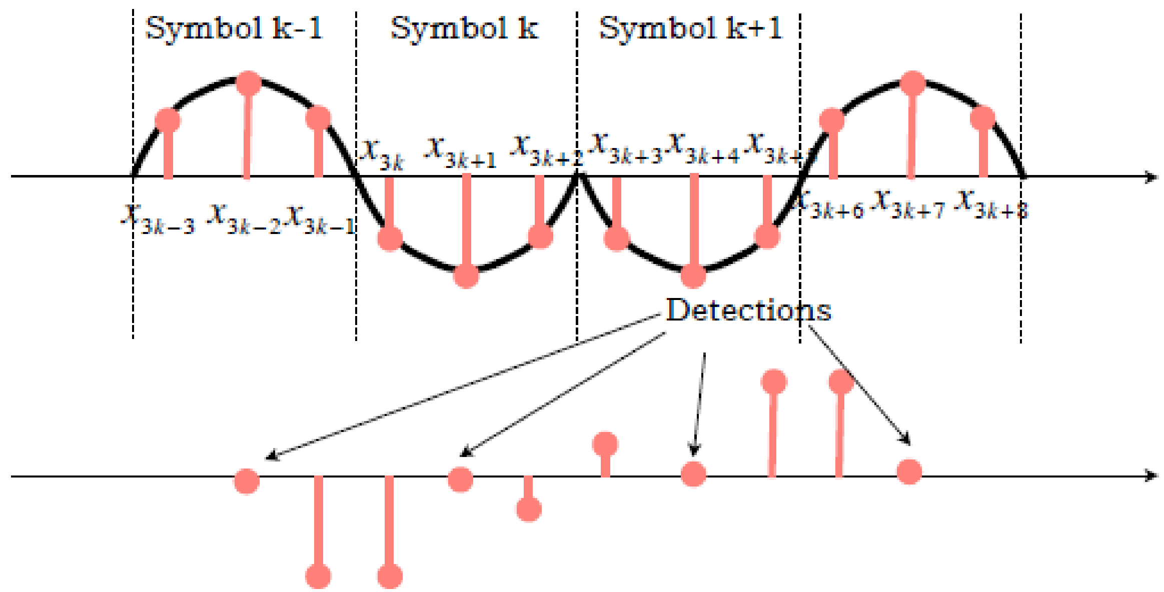
- For BPSK or QAM signals
- 2 samples/symbol



- The sums $y_k = x_k + x_{k-1}$ are calculated
- When y_k is small, but not zero
  - A time correction proportional with y_k is applied

Early-late recovery

- 3 samples/symbol



- The middle of the symbol is detected

$$y_k = x_{k+1} - x_{k-1}$$