Frequency Synthesis

5.1 General information

- Frequency synthesizers - complex systems — by means of which we can generate sinusoidal signals with the necessary frequency for a certain aplication, starting from one or more *Reference Oscillators (RO).*

- Initially, the operation of a synthesizer consisted in :
  - choosing the output of an RO from several;
  - changing the quartz crystal used to control the frequency of the oscillator.

- Later more complex models were conceived, trying to achieve the following objectives:
  - Generating as many frequency values as possible, starting from a small number (as small as possible) of reference oscillators;
  - Generating a signal as pure as possible from the spectral point of view;
  - The parameters of the generated signal must become stable as fast as possible after the start of the synthesizer or after the change of the frequency value.

- Keeping in mind the above mentioned aspects, the most important parameters of a synthesizer are:

  - The frequency range;
  - The synthesis frequency step (the space between two successive frequency values of the generated sinusoidal signal);
  - Spectral purity;
  - Settling time;

- A first classification of frequency synthesizers may be done taking into account the method used to process the reference signal;
- So, we can distinguish synthesizers that use:

  a) direct methods of processing;

  b) indirect methods of processing.

a) Direct methods

- These methods use combinations of sinusoidal signals generated by several reference oscillators or of harmonics of these signals by means of multiplication, division, mixing, filtering;

- In turn, these synthesizers can be:

  - Analogic
  - Digital

- Analogic synthesizers – which are becoming more and more rarely used, need to make a compromise between:
  - High spectral purity – very selective band-pass filters are necessary;
  - Low settling time – less selective filters are necessary.
- Digital synthesizers will be presented in this chapter, for they are a modern and very efficient solution, if the generated frequency is not very high.

b) Indirect methods

- They are based on PLL circuits:
  - analogical
  - digital
- The signal is generated by controlling the OCT frequency, so the problem of intermodulation products is eliminated.
- Still, the need to make a compromise is still present;

- The two contradicting requirements are:
  - the exploration step of the frequency range
  - the settling time

- These parameters can be controlled by means of the pass- band of the loop filter (LPF);

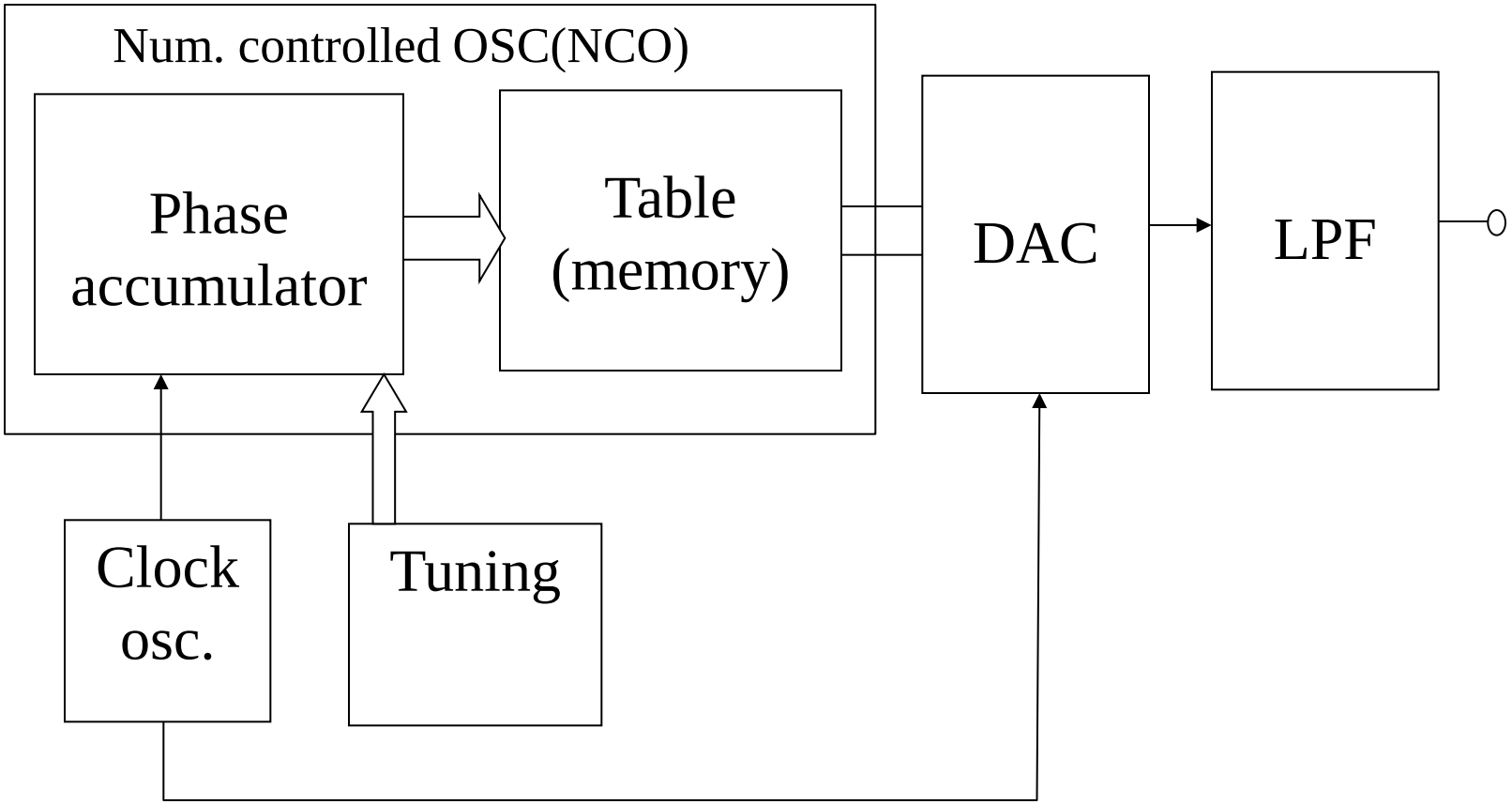
5.2 Direct digital synthesis

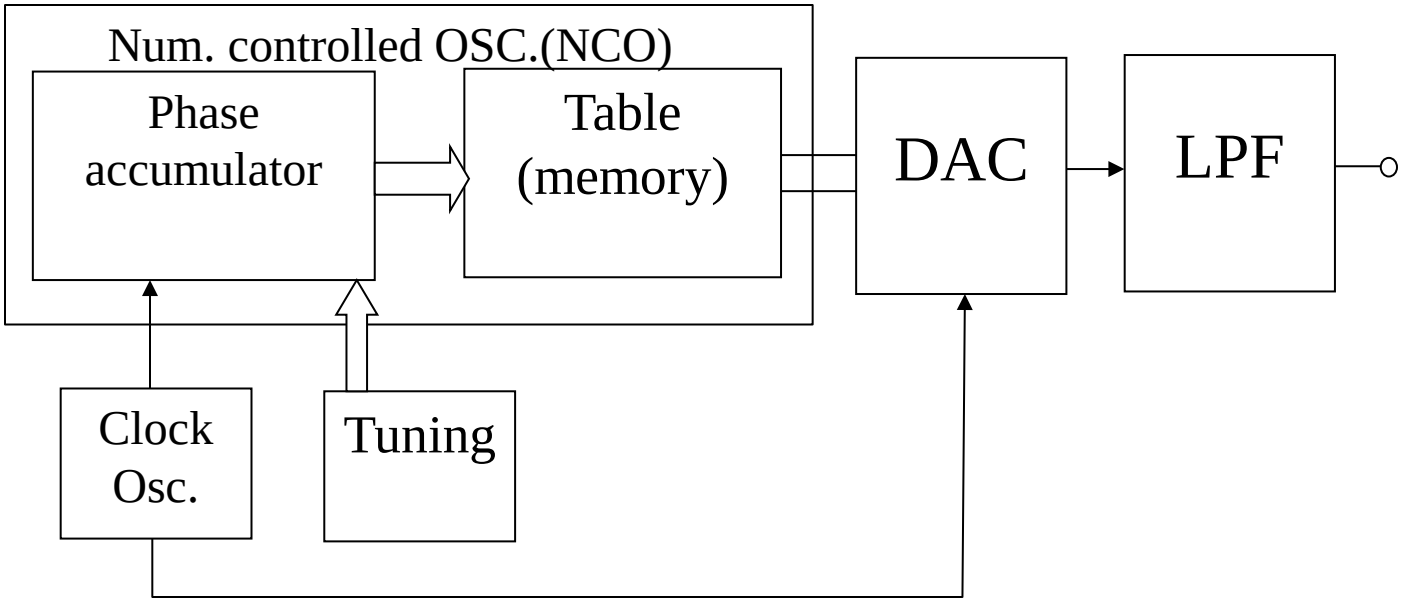
- Analogic synthesizers may contain: multipliers, filters that require tuning, PLL circuits, OCT circuits, temperature drift compensation circuits, components selected via measurement, etc.

- Digital synthesizers require only logical circuits, and a clock oscillator.

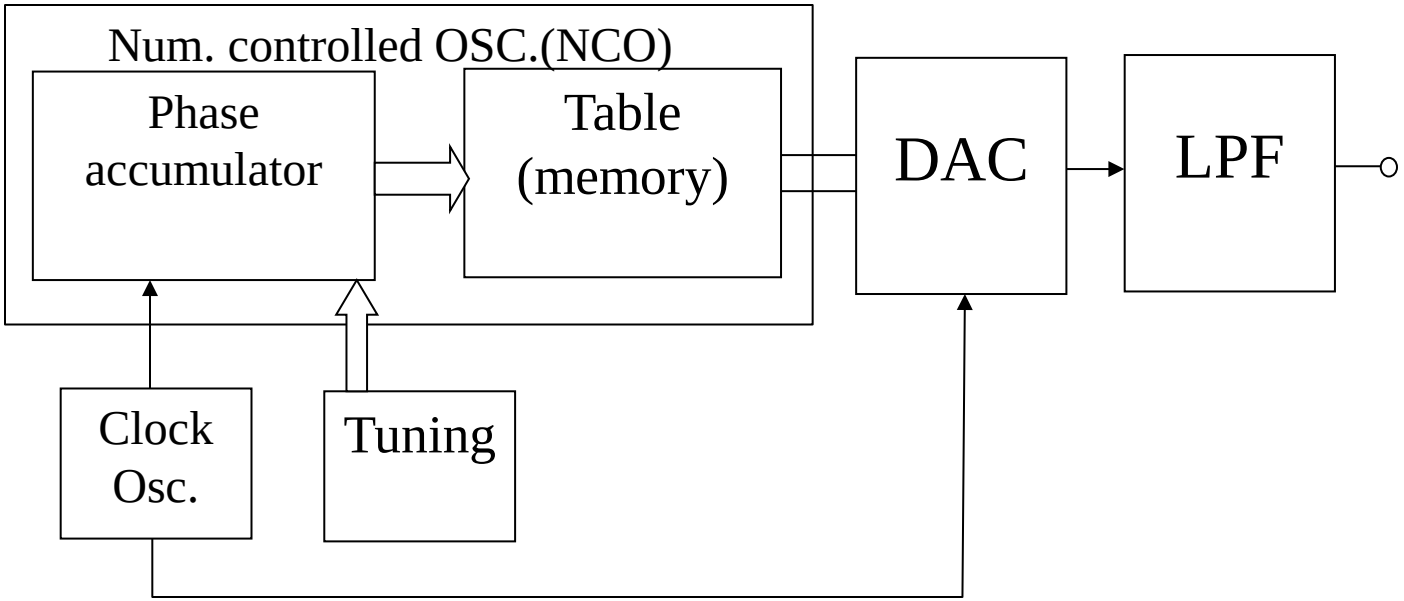
- The main advantages that make this syntesis method very tempting are:
  - repeatability
  - reliability
  - absence of tuning circuits
  - absence of circuits that reduce temperature drift or time drift.
- Digital synthesizers still have some limits regarding the maximum frequency they can generate.

➢The block diagram of a direct digital synthesizer:





- We can notice that the block diagram contains three important blocks:
  - The numerically controlled oscillator (NCO)
  - The digital-analog convertor (DAC)
  - The output filter useful to suppress the high frequency components.

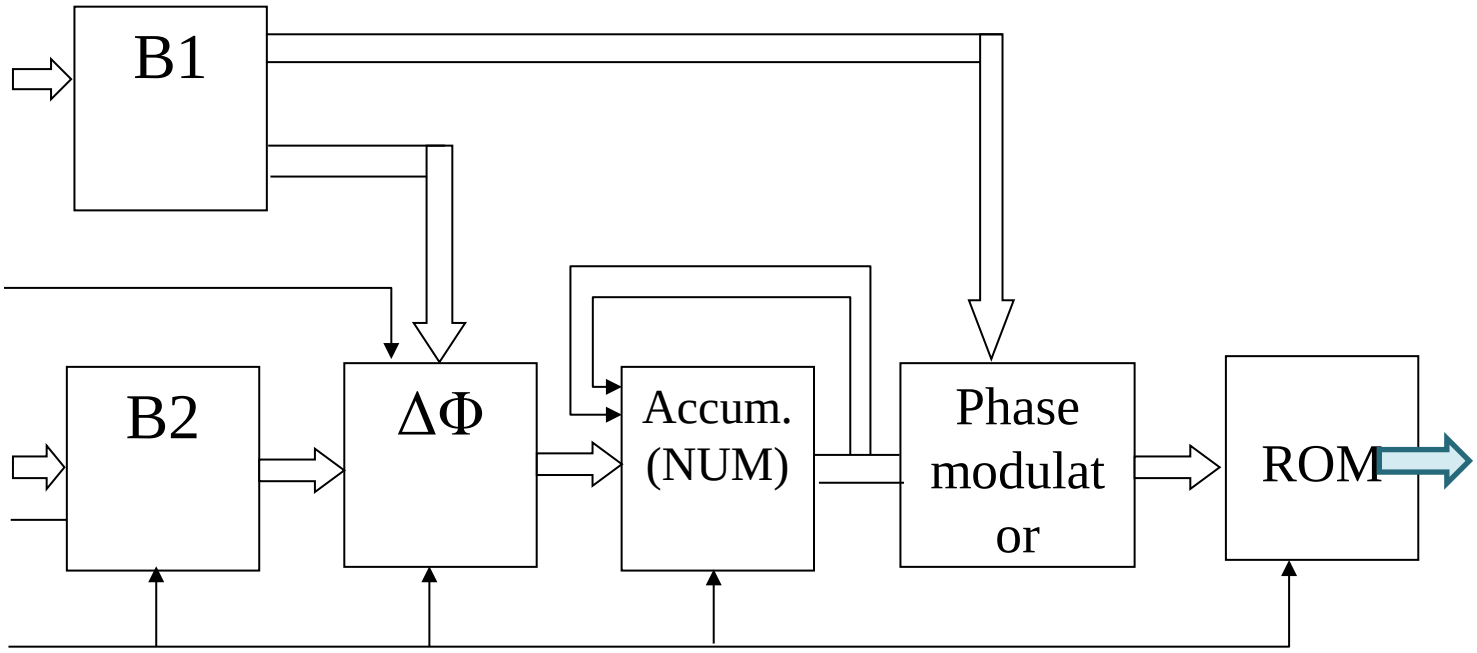


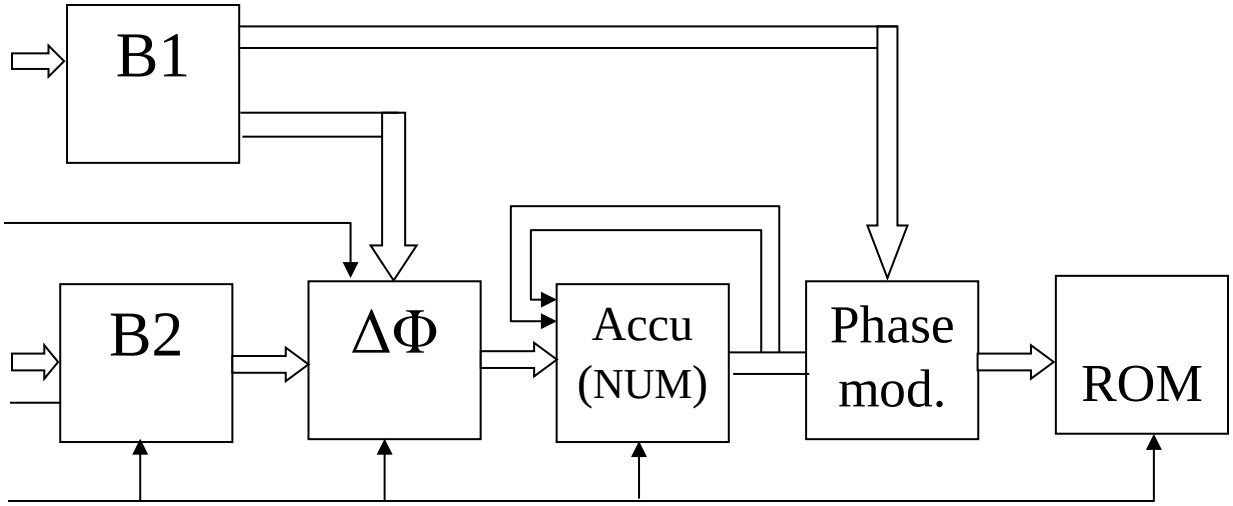
➢ Among the input parameters, we can remark:

- The reference frequency (clock) that increments the counter and inserts new information in the convertor;
- The control data for the frequency value and for controlling the modulation.

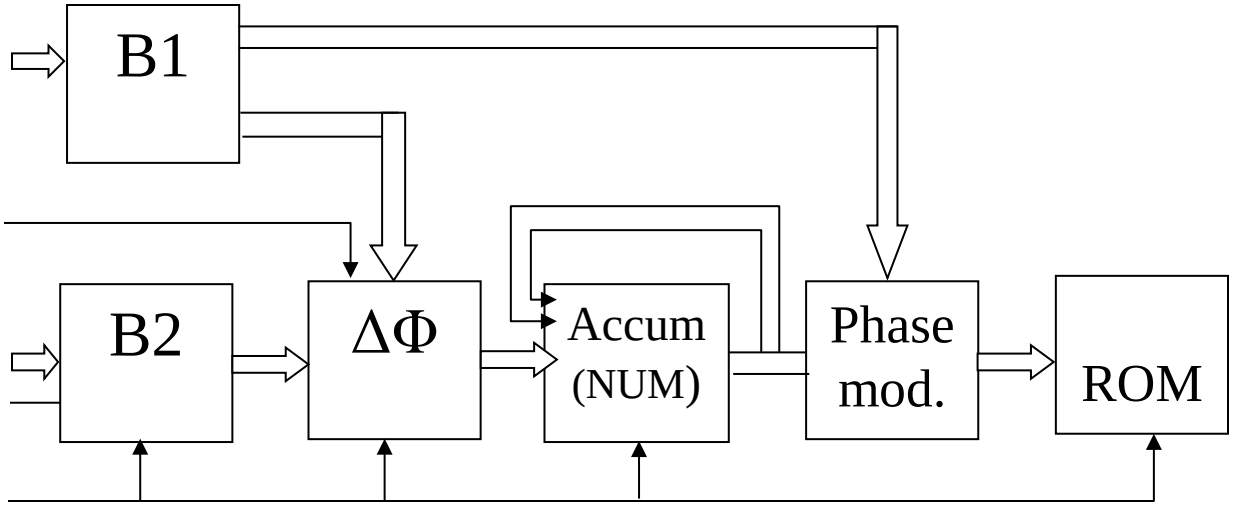
- Next we will go into detail regarding some of the bulding blocks;

5.2.2. Numerically controlled oscillator

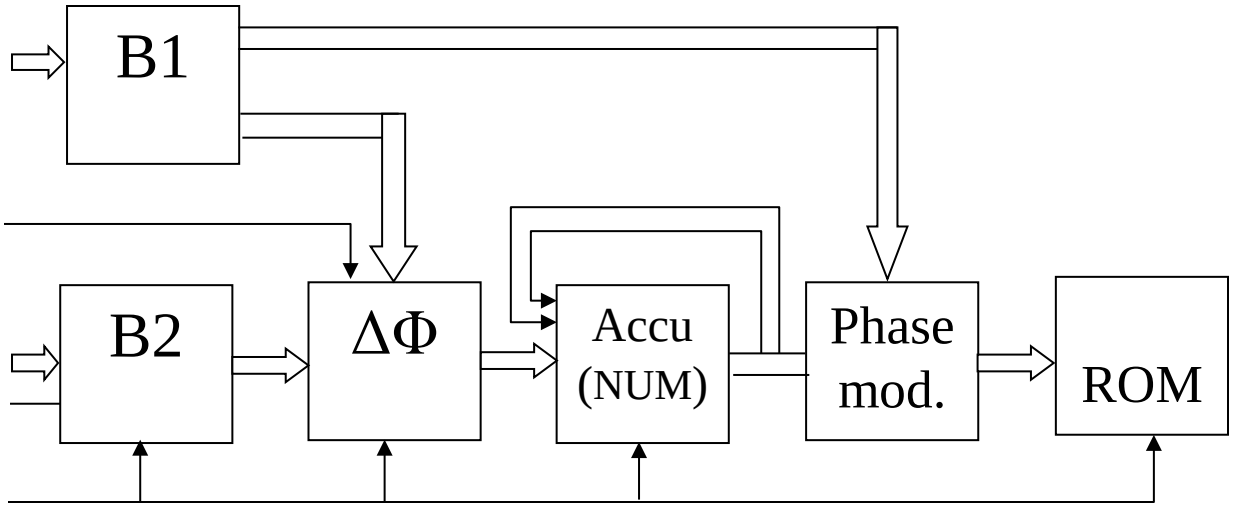




- The numerically controlled oscillator contains:
  - Interface logic;
  - Phase accumulator, which is, in fact, a counter;
  - A table (ROM) in which the samples for the generated waveform are stored.



- The B2 buffer allows for inserting a word that controls the value of the frequency.
- Every clock pulse increments the counter with a value given by the above mentioned word (step) denoted by ΔΦ;
- A linear increase in phase is performed, so that it may correspond to a sine signal.



- It is easy to realize that the frequency represented by the linearly increasing phase depends on:
  - The clock frequency applied to the phase accumulator;
  - The value of the phase step;
  - The maximum value of the counter;

$$f_{out} = \frac{f_t \cdot \Delta\Phi}{2^m}$$

- Here, ***m*** represents the number of bits of the counter (phase accumulator)
- So, the value of the frequency may be modified by controlling $\Delta\Phi$.
- The linearity of the phase variation, thus the spectral purity of the generated signal depends (most importantly) on the spectral purity of the clock signal.

- This synthesizer is, in fact, a frequency divider, so the phase noise of the generated signal will be smaller than the noise of the clock oscillator

$$f_{out} = \frac{f_t \cdot \Delta\Phi}{2^m}$$

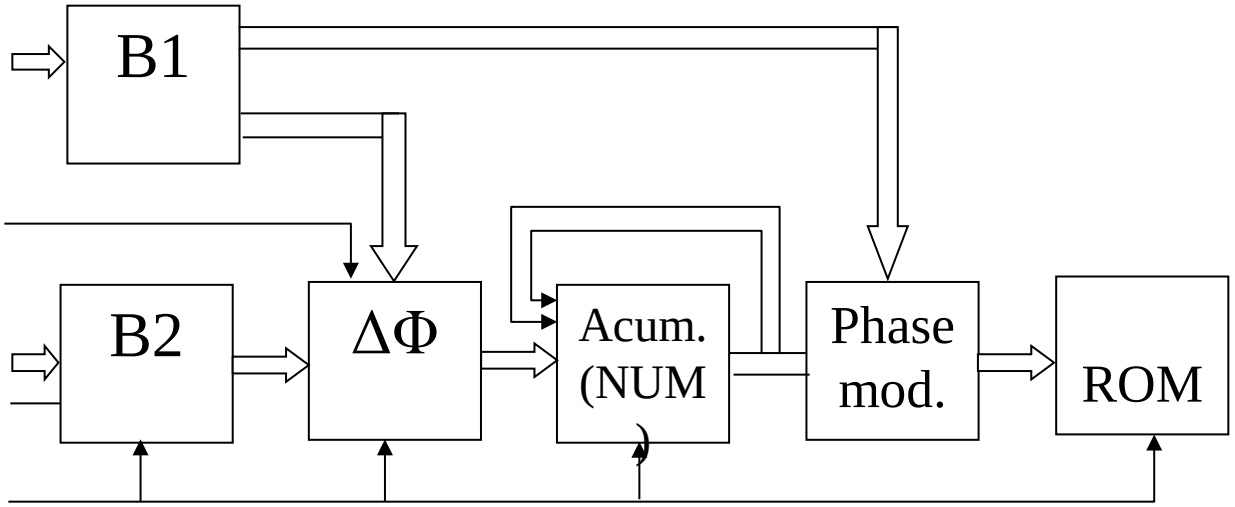
- Obviously: f_t and m are constant parameters in a synthesizer.
- They are chosen according to the frequency range that must be covered (f_{max}) and the step (δf) with which this range must be explored.

- We notice that:

$$f_{max} \cong 0{,}4 f_t \qquad \delta f = \frac{f_t}{2^m}$$

- The first limit results from the sampling theorem (the input signal must be sampled with a frequency larger than double of the maximum frequency in the spectrum).

- From the second relation, it is obvious that it is possible to realize small frequency steps, if the phase accumulator ensures a sufficient resolution.



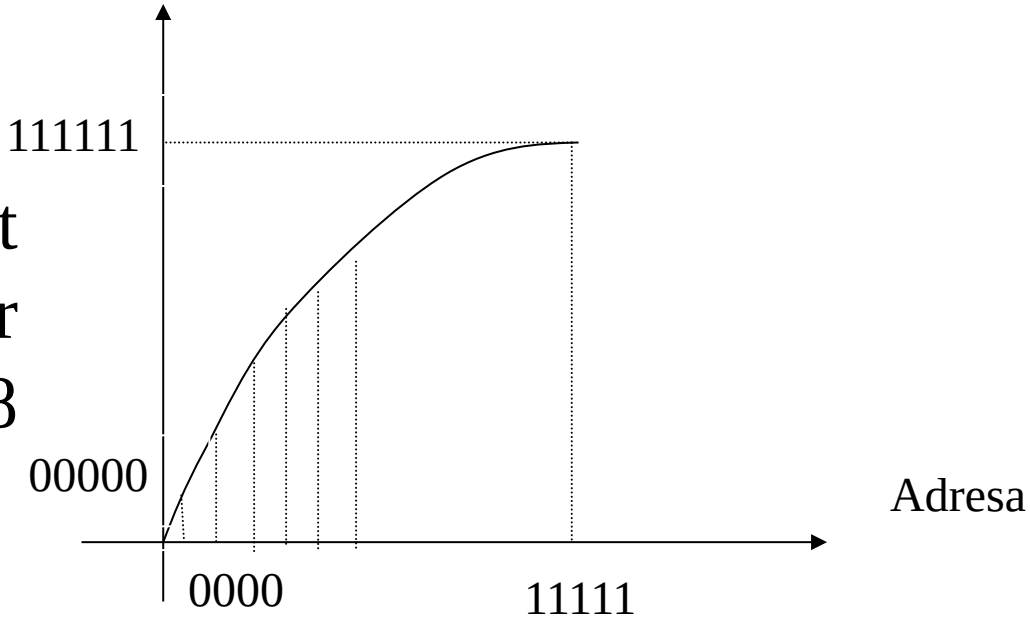
- The operating method of the accumulator accentuates the fact that from the moment it is charged with a new step, the phase begins to vary according to the new step value;
- So, frequency modulated signals may be easily generated, just by changing ΔΦ.
- One can remark that continuous phase frequency modulated signals are obtained.

5.2.3. The Memory

- Phase-amplitude conversion may be done by reading the value inscribed at the correspondent memory address (ROM).
- Any periodical signal with a linearly increasing phase has a biunique correspondence between amplitude and phase;
- It may be generated by reading the values of the samples calculated and inscribed in the memory (at the right time);

- Aspects specific to sine signals allow for the reduction of the necessary memory;

- We remark the fact that the counter may have up to 48 bits.



- Usually the other blocks use only the most significant (10-12) bits, the resolution being sufficient.

Conclusions regarding the spectral purity

- The phase noise does not represent a problem;
- However, parasitic components appear due to the quantization noise and the imperfections of the converter;
- The place where these components appear is predictible, but their amplitude is not;

- Signals of frequencies up to 1 GHz can be generated using DDS synthesizers;
- So: $f_0 \leq 400\text{MHz}$.

5.2.4. Conclusions

- Synthetically speaking, we may remark the following aspects specific for a DDS:

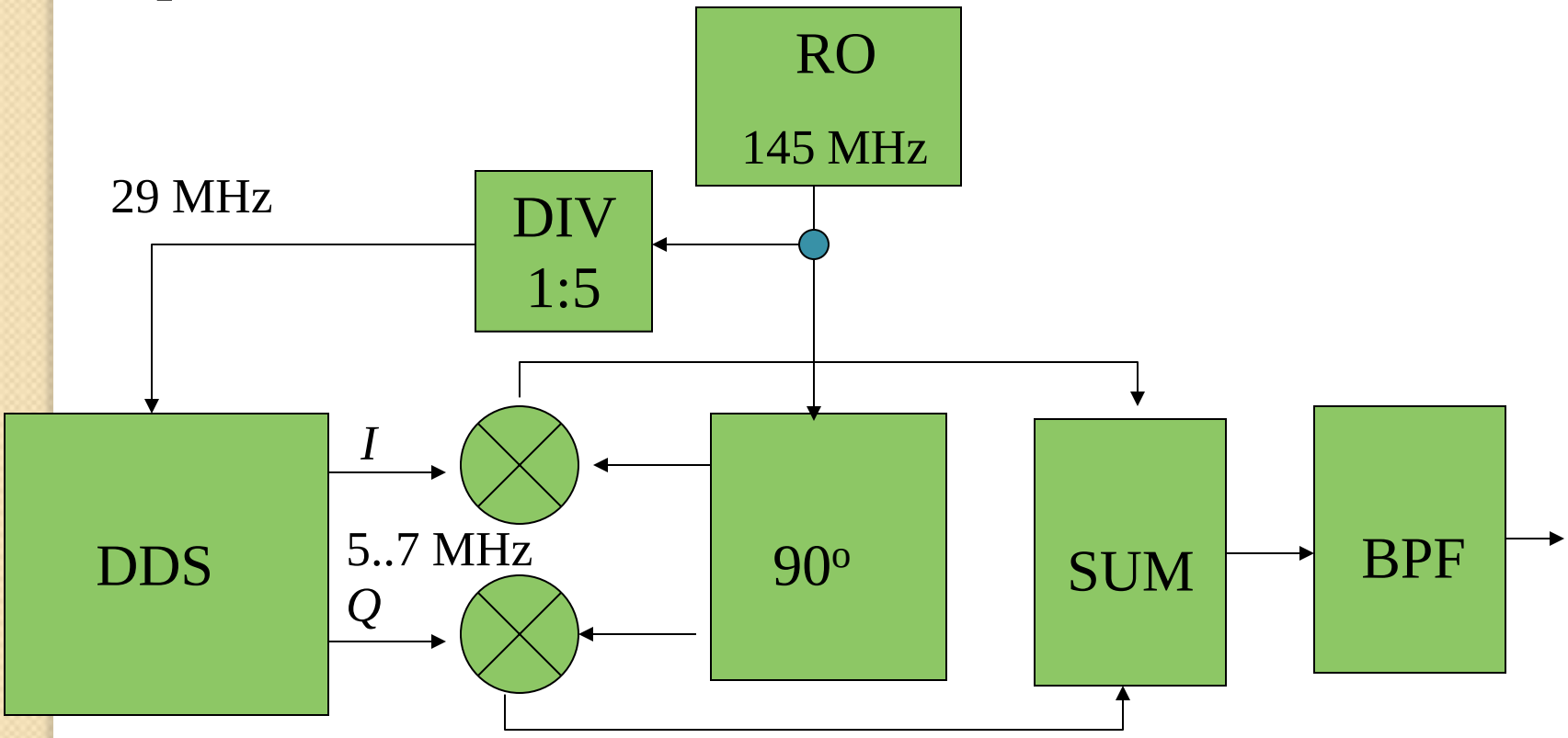
- small work regime settling time (under 1 μ s)
- fine or very fine resolution (< 1 μHz)
- may process over several octaves;
- continuous phase frequency modification;
- very linear analogic/data modulation (typically 16 bits)
- ;

5.2.5. Applications

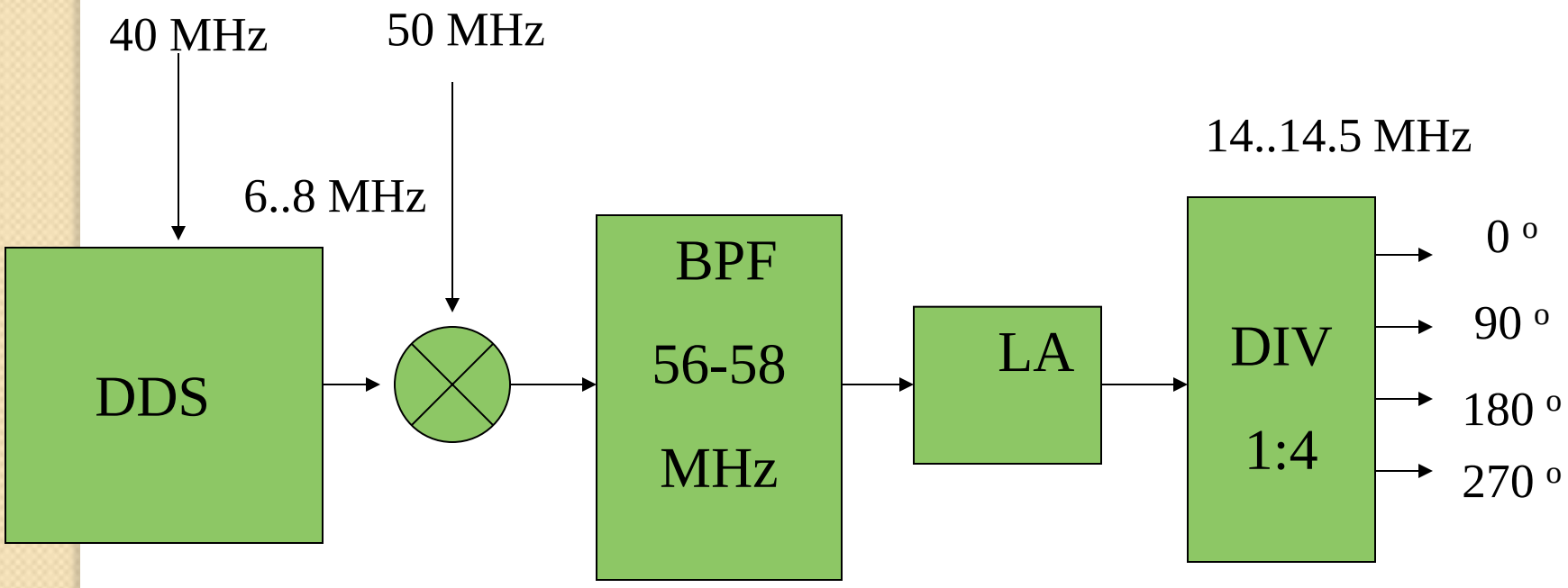
- Scattered spectrum radio equipment (DS or FH)
- Doppler radars
- Generation of high-speed or fine resolution digital frequency modulation (FSK) or digital phase modulation (PSK);
- Radio broadcasting or radio television equipment (DAB, DVB, HDTV);
- Laboratory equipment;
- Magnetic resonance visualization equipment.

5.2.5. Examples of DDS synthesizers

1. Synthesizer *in the range of 150..152 MHz, 1 Hz resolution, stabilization time of 1 us, undesired components -65 dBc*;



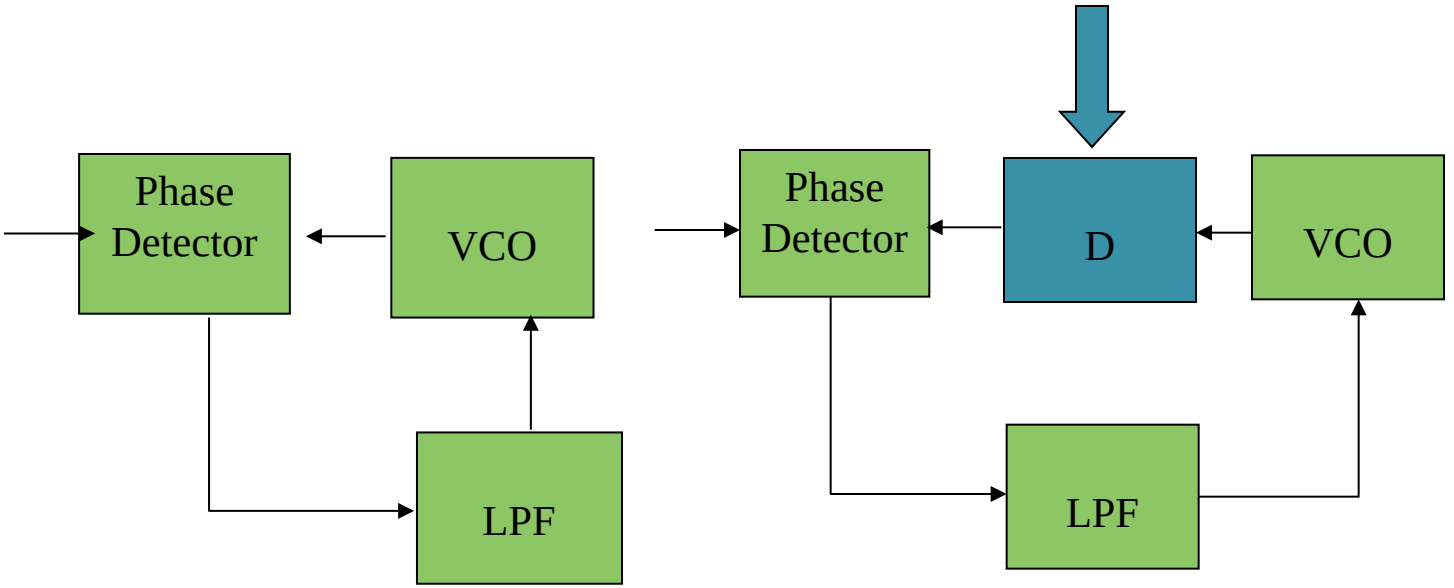
2. Synthesizer *in the range of 14..14.5 MHz, resolution of under 10 Hz, stabilization time of 10 us, undesired components -80 dBc, phase noise -100dBc, 4 components shifted to 90 degrees with errors smaller than 1° ;*



5.4 Frequency synthesis realized using digital PLL circuits (DPLL)

5.4.1 DPLL specific aspects

- PLL and DPLL block diagram:



- Differences between the two choices can be found in:

a) the type of the building blocks;

b) the functioning of the circuit;

c) the achieved performance;

d) applications.

a) The type of the building blocks:

- processed signals are square wave signals;
- digital circuits with known advantages are used in.

Phase detection

- in analog PLL's, we use an Analog Multiplier (AM) with a sine characteristic:

$$u_e(t) = k \sin(\varphi_2 - \varphi_1) = k \sin \varphi_e(t)$$

- Making DP's with other performances is easy to accomplish in digital technique;

➢ Programmable divider

- using a frequency divider (programmable divider) in the loop, on the feedback path, extends the area of applicability of the DPLL;

b) Differences in the sense of functionality

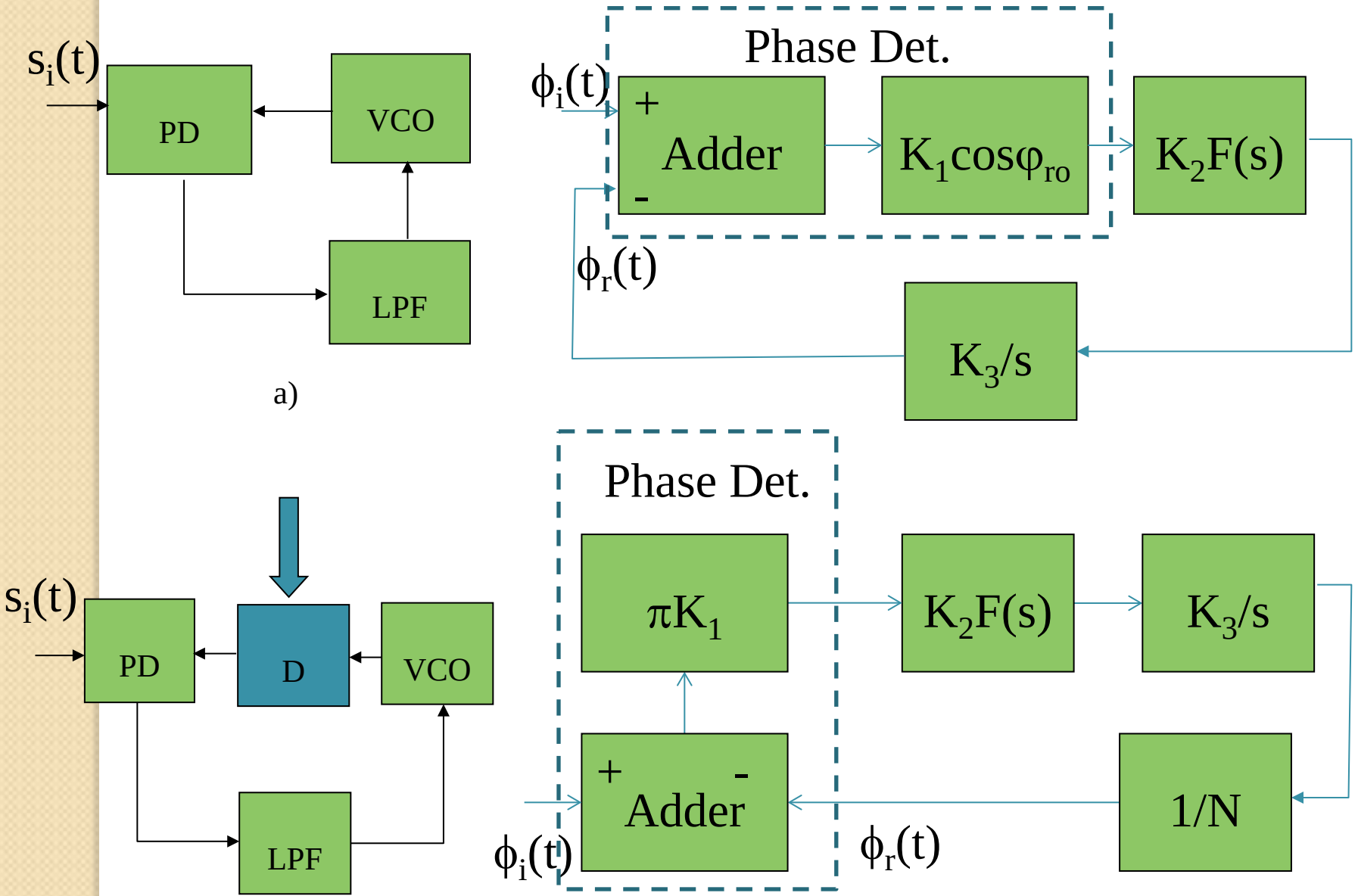
➢consequences of the previous ones;

➢for example, the structure of the signals delivered by the phase detector and

➢ the effect of this PD and of the programmable divider on the LPF requirements ;

c) Equivalent block diagrams that allows for evaluation of performance related differences are given on the next slide;

- These block diagrams was obtained considering that the PLL circuit in the synchronism regime;


$s_i(t)$
PD
VCO
LPF
a)
Phase Det.
$\phi_i(t)$
+
Adder
-
$K_1\cos\varphi_{ro}$
$K_2F(s)$
$\phi_r(t)$
K_3/s
$s_i(t)$
PD
D
VCO
LPF
b)
Phase Det.
πK_1
$K_2F(s)$
K_3/s
+
Adder
-
1/N
$\phi_i(t)$
$\phi_r(t)$

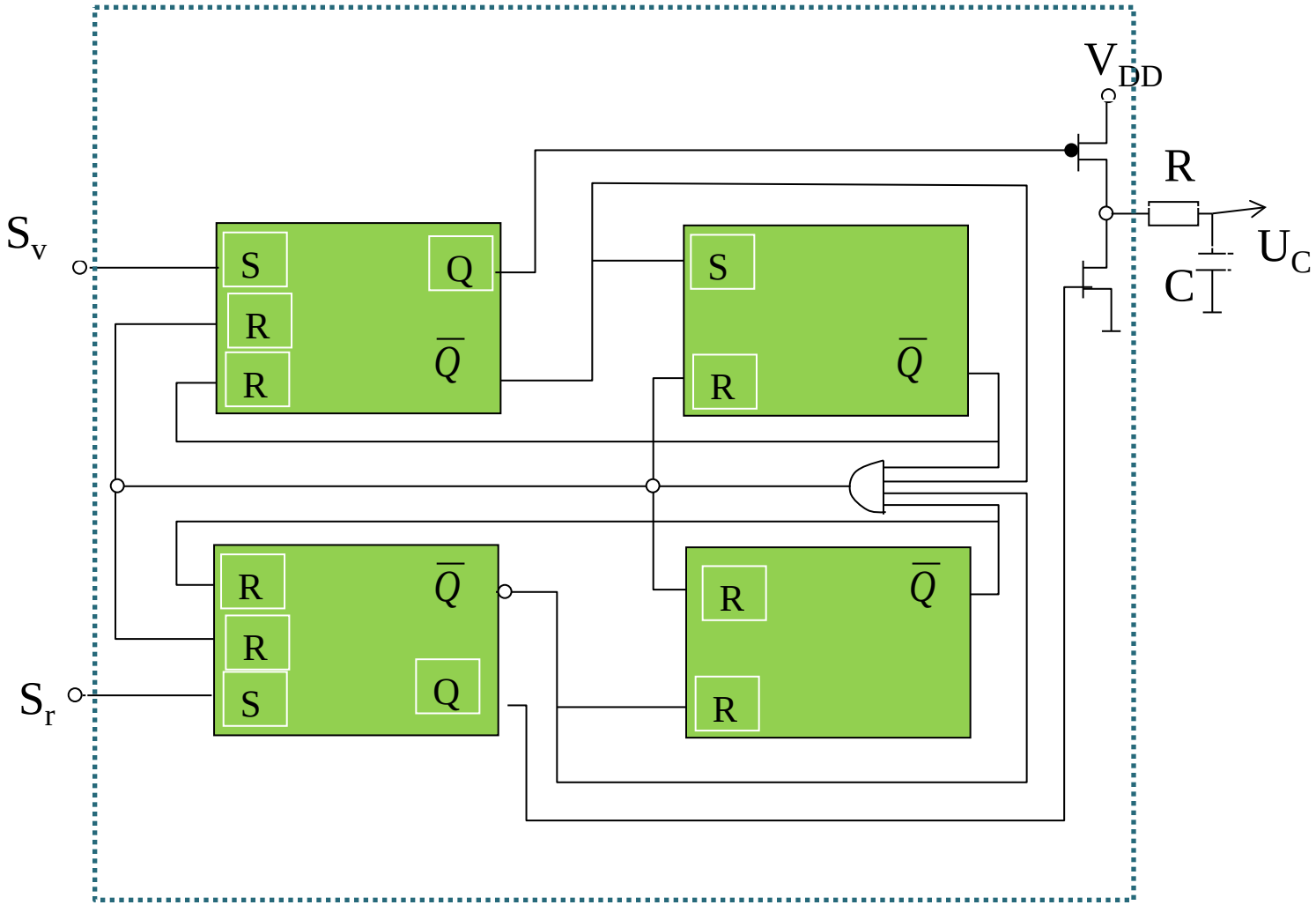
d) Applications

- APLL: mainly – demodulation;
- DPLL: mainly - frequency synthesis.

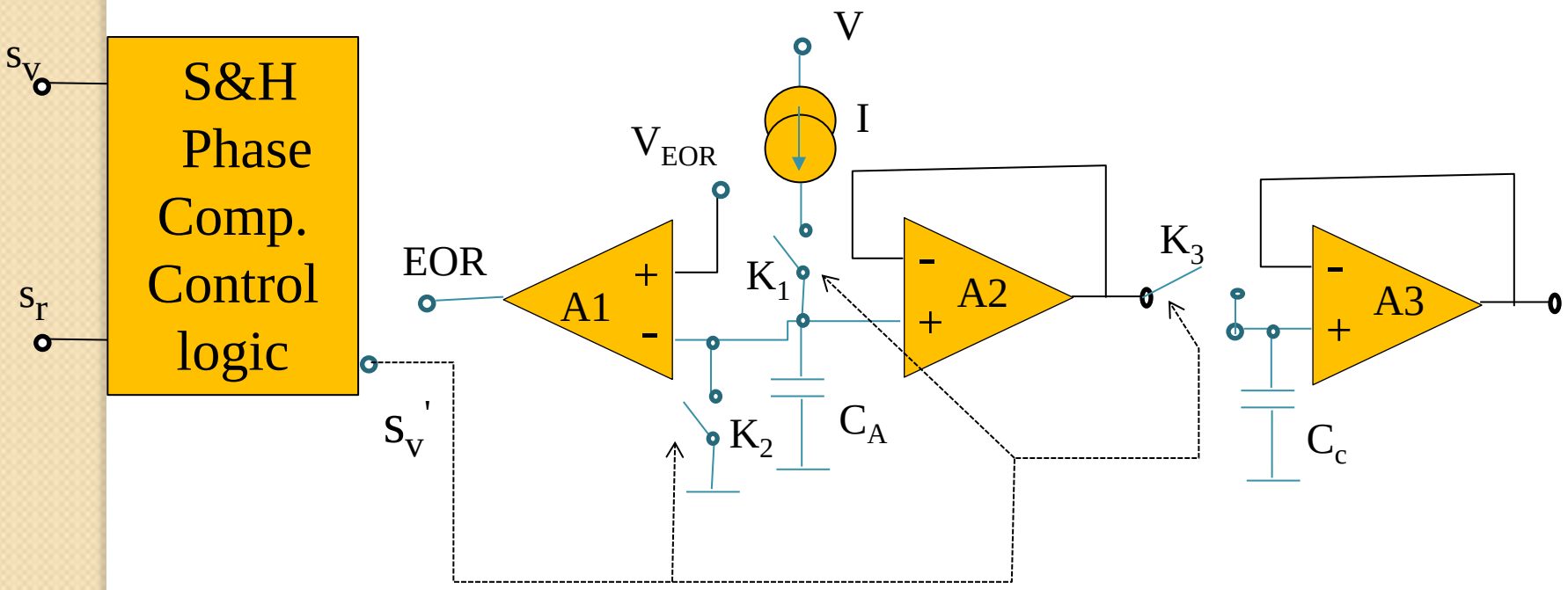
5.4.2 Phase detectors (comparators) used in creating DPLL circuits

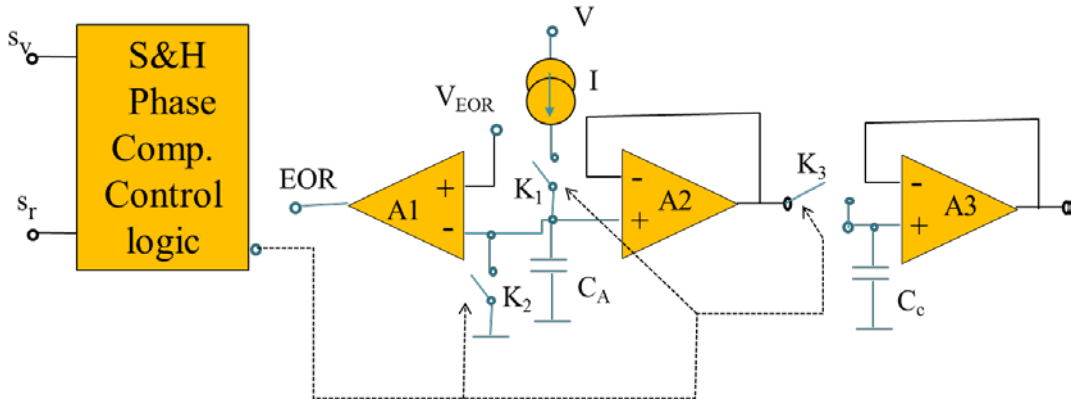
- The correspondent to the Analog Multiplier used in analog PLL – a XOR circuit (exclusive OR, modulo 2 adder) – disadvantages;
- Digital phase detectors;
- SAMPLE&HOLD phase detector;
- The input signals of the phase detector: $s_r(t)$ and $s_v(t)$;

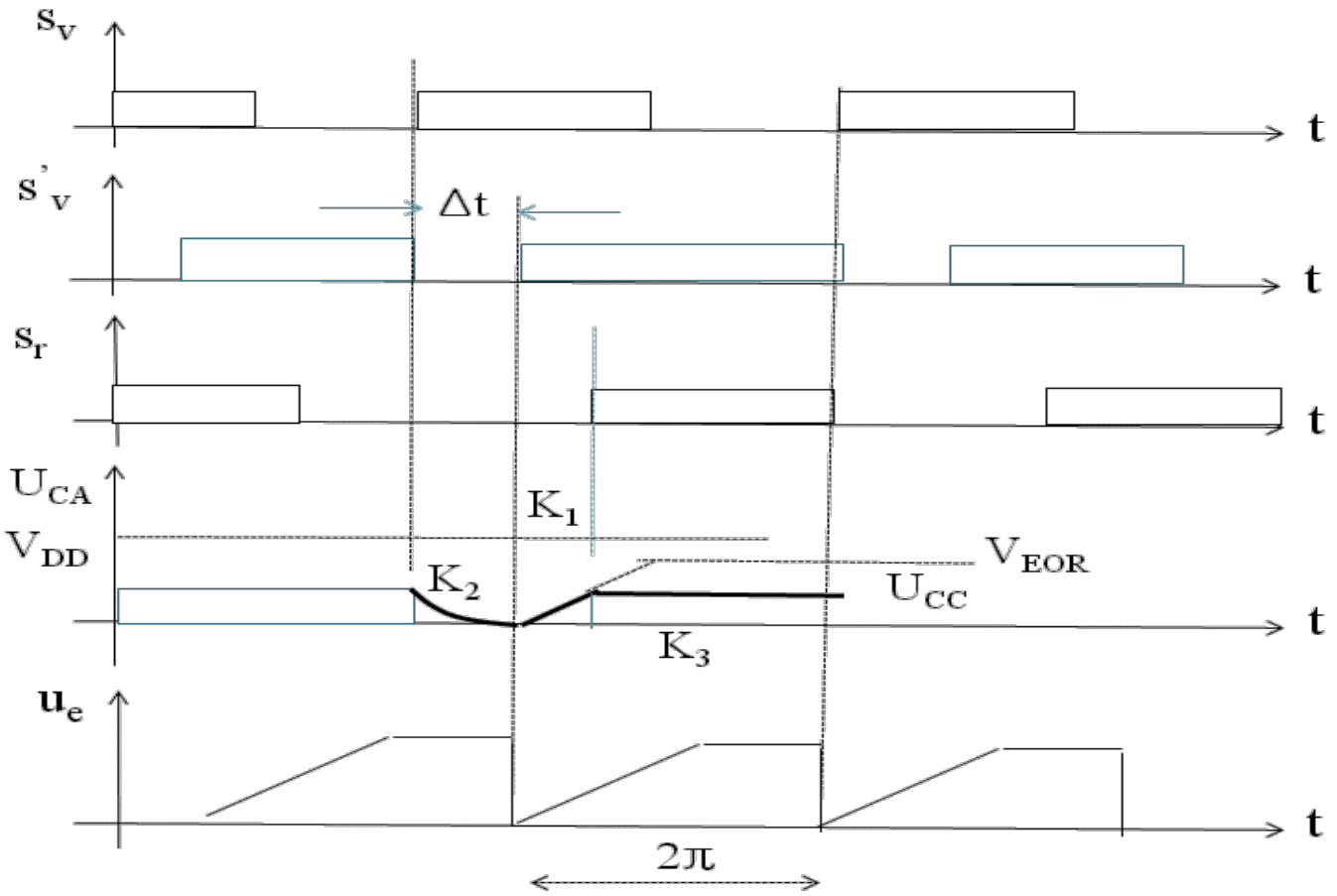
➢A digital phase detector based on RS bistable circuits:



➢ SAMPLE & HOLD phase detector:

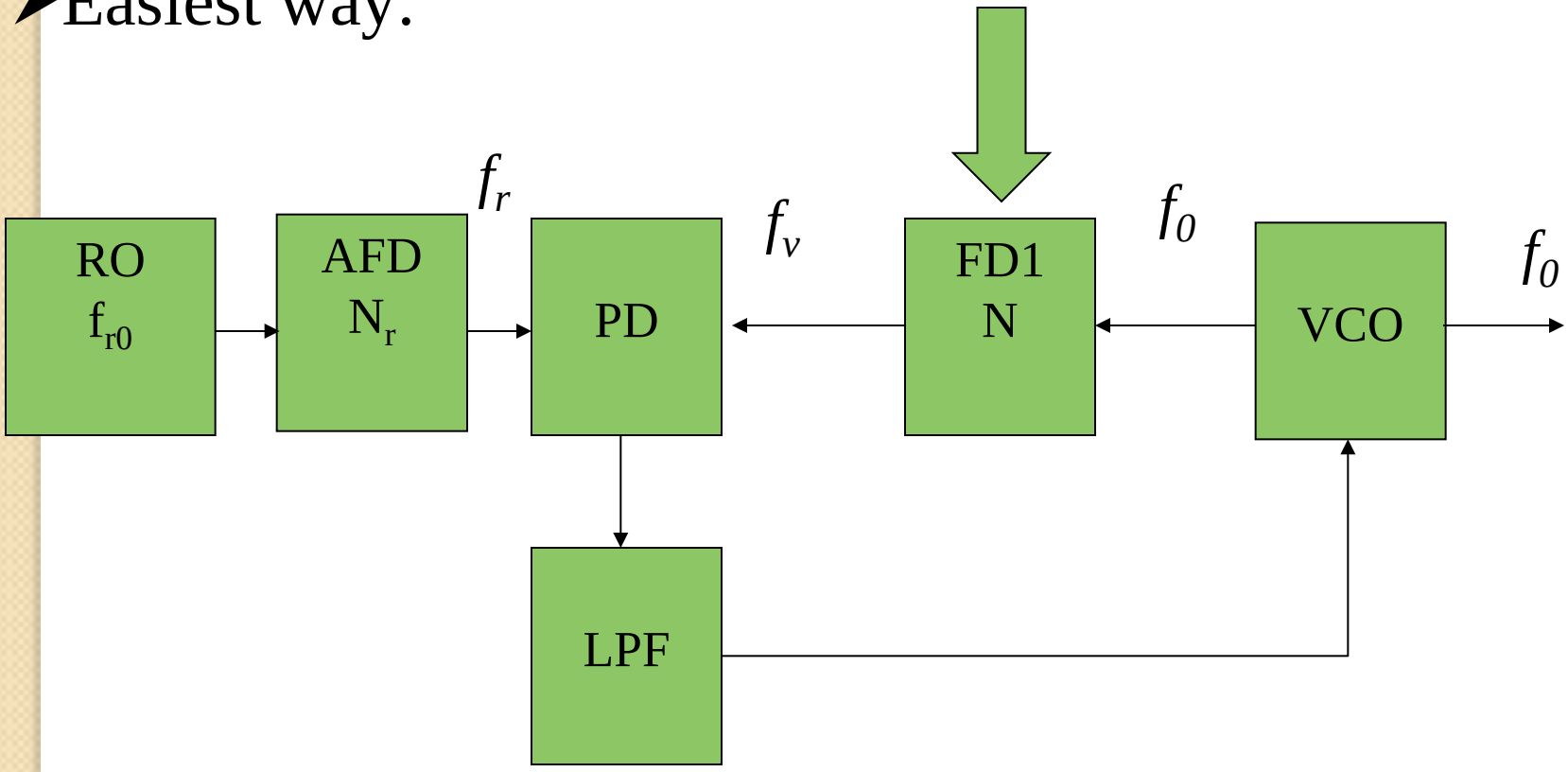



S&H
Phase
Comp.
Control
logic
V
I
V_EOR
EOR
A1
A2
A3
K1
K2
K3
C_A
C_c


s_v
t
s'_v
Δt
s_r
U_CA
V_DD
K1
K2
K3
V_EOR
U_CC
u_e
2π

5.4.3 DPLL frequency synthesizer

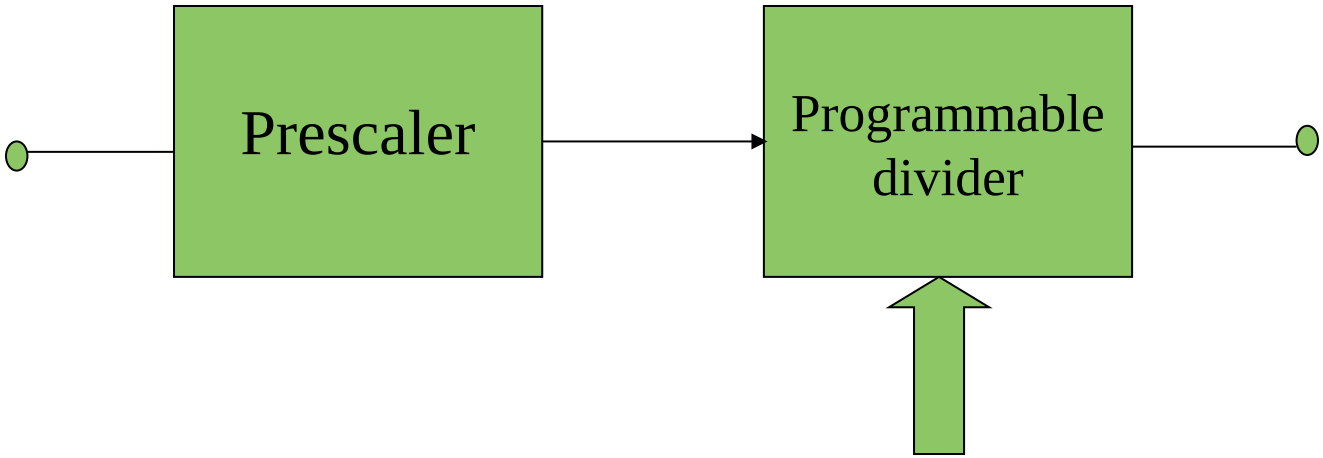
- Easiest way:

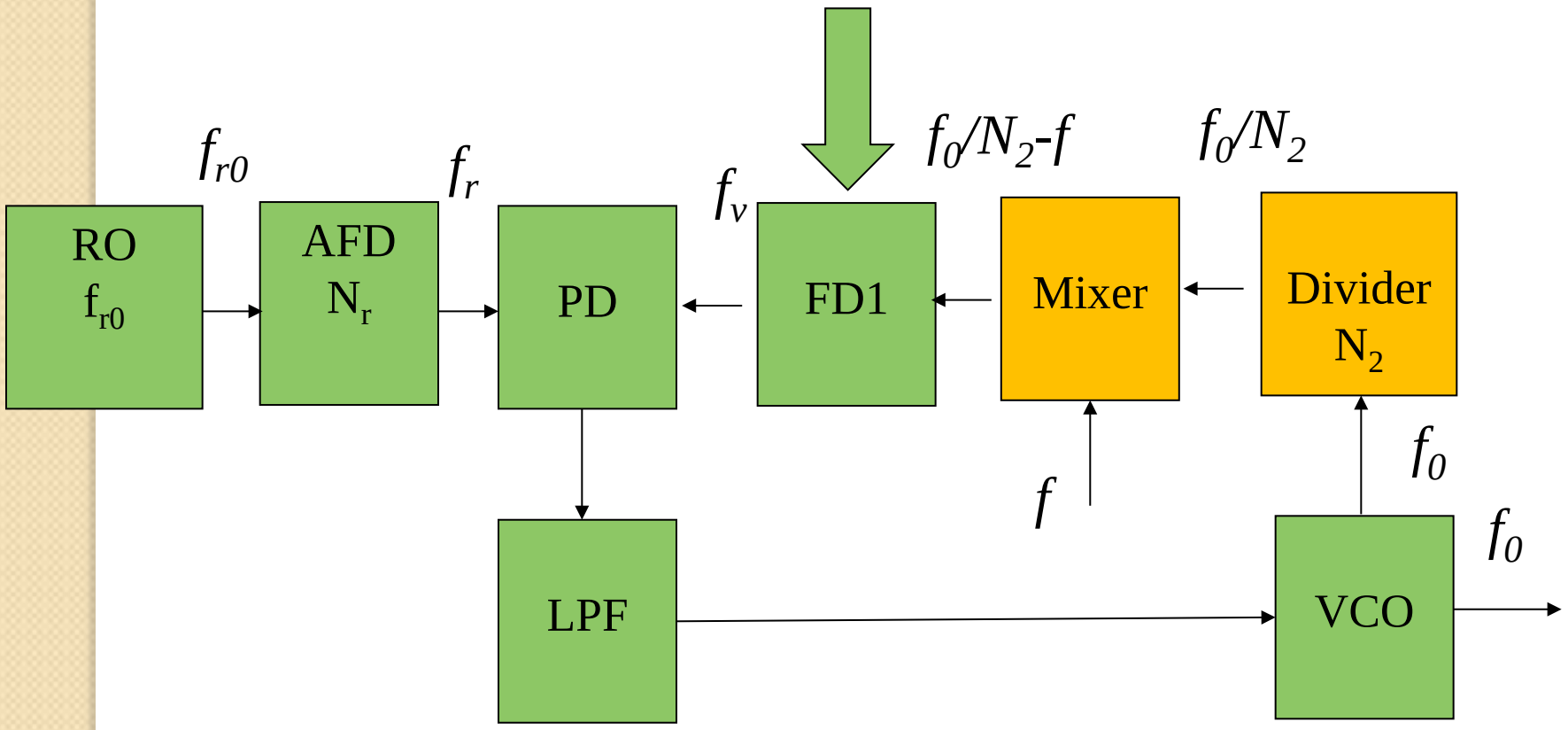


$$f_0 = N \; f_r$$

Programmable dividers

- CMOS – 5 MHz
- TTL (20-40) MHz.

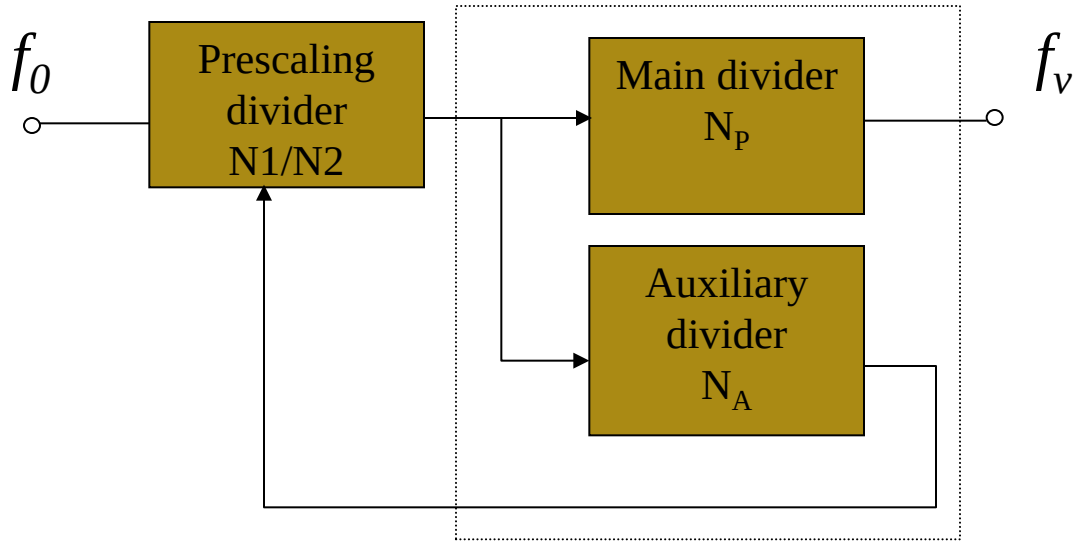




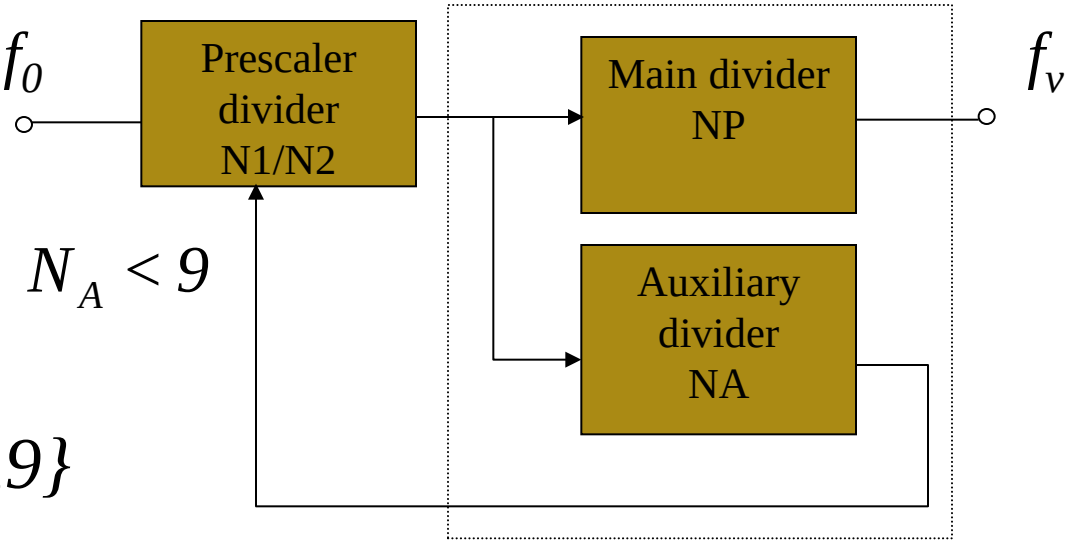
$$f_v = \frac{1}{N}\left(\frac{f_o}{N_2} - f\right) = f_r; \qquad f_o = (N f_r + f) N_2$$

- step becomes $N_2 f_r$

- In order to avoid the unwanted increase of the step, we may use prescaling dividers (prescaler) that can be controlled (fractional dividers) (not programmable);



- We will analyze the case of a 10/11 divider



$$N_p = \sum_{m=1}^{M} A_m 10^{M-m};\ N_A < 9$$

$$A_m, \in \{0,1,..,9\}$$

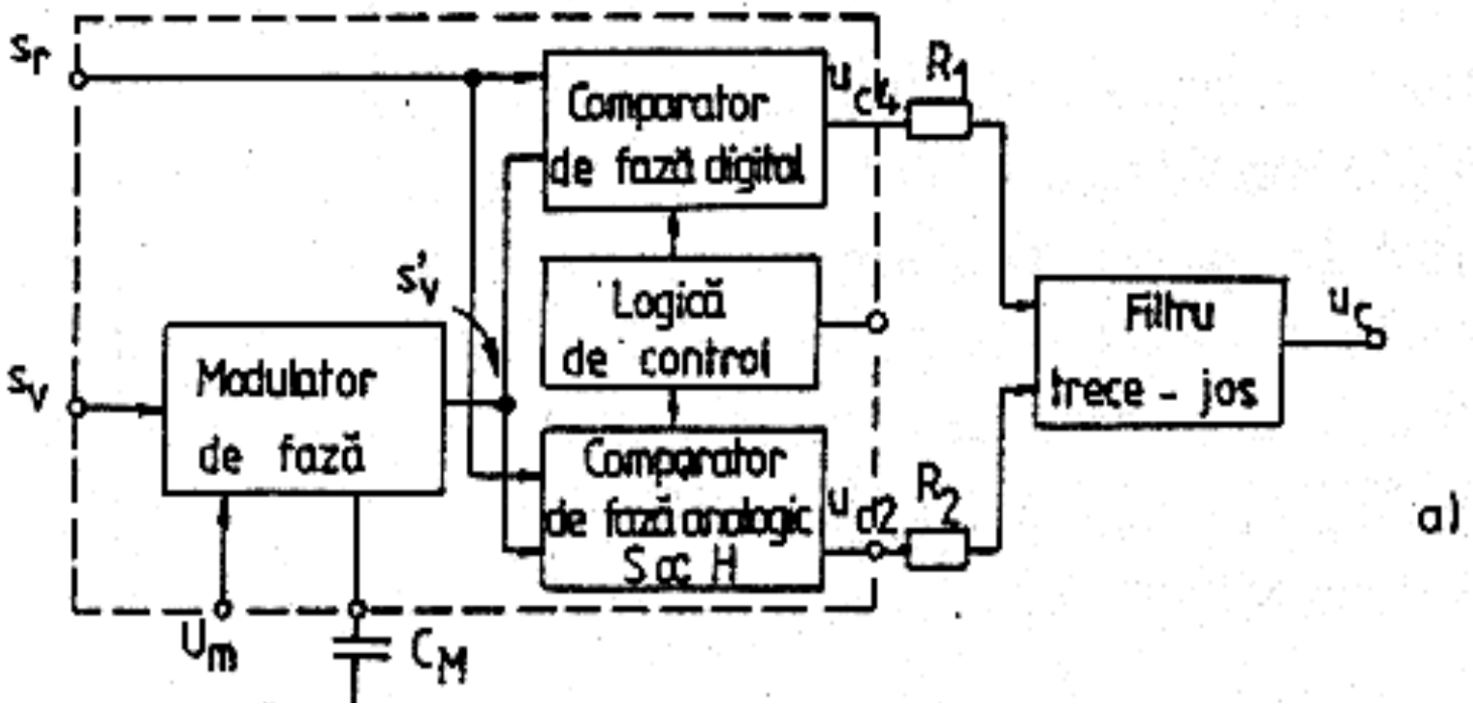
- If, for example, the prescaler has a fixed coefficient N_2=10, it results:

$$f_o = N f_r = N_P f_r N_2 = f_r \sum_{m=1}^{M} A_m 10^{M-m+1}$$

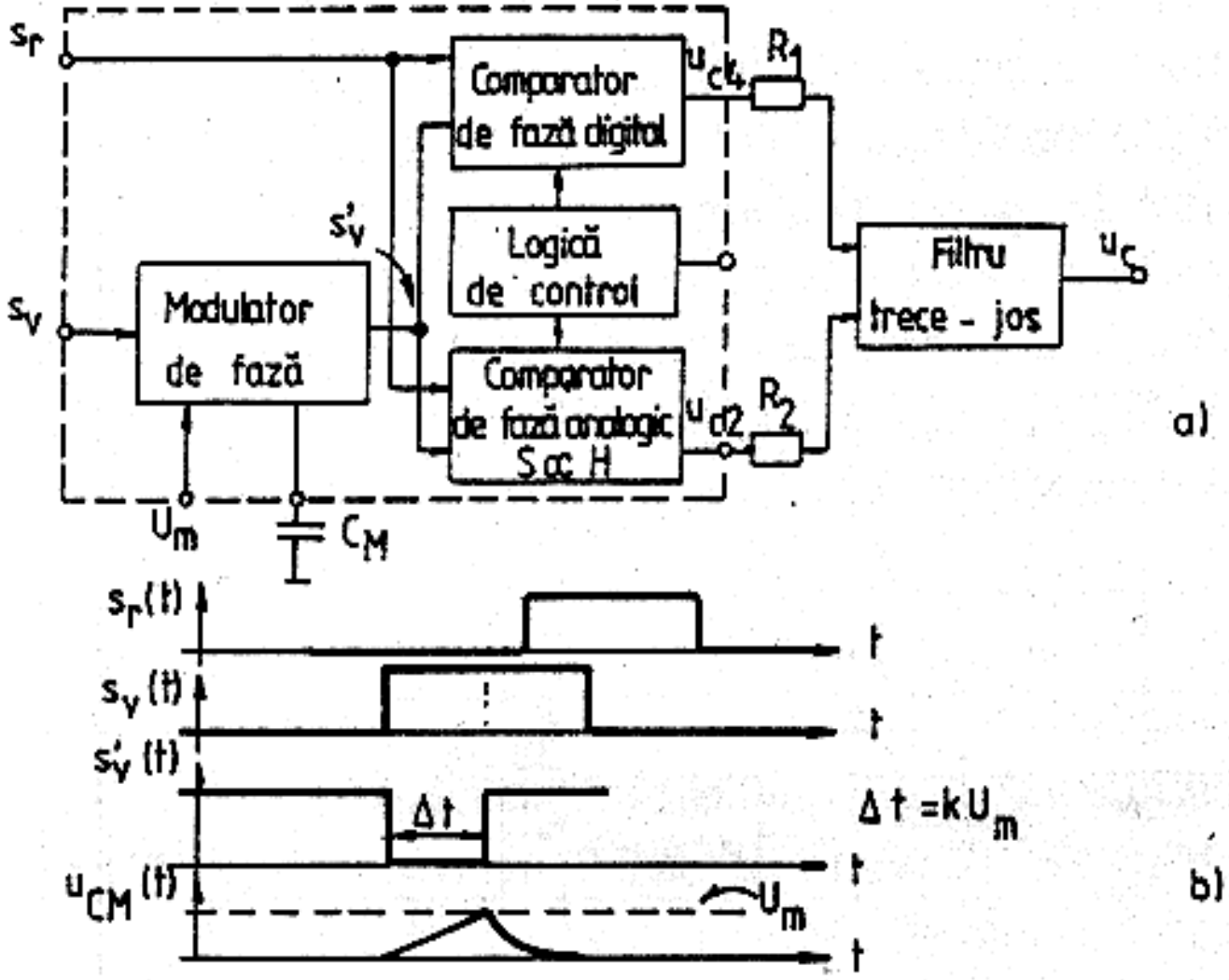
- In the analyzed case:

$$N = 11 N_A + 10[\sum_{m=1}^{M} A_m 10^{M-m} - N_A] = \sum_{m=1}^{M} A_m 10^{M-m+1} + N_A$$

- Another aspect: reducing the parasitic phase modulation due to the harmonic components of f_r;

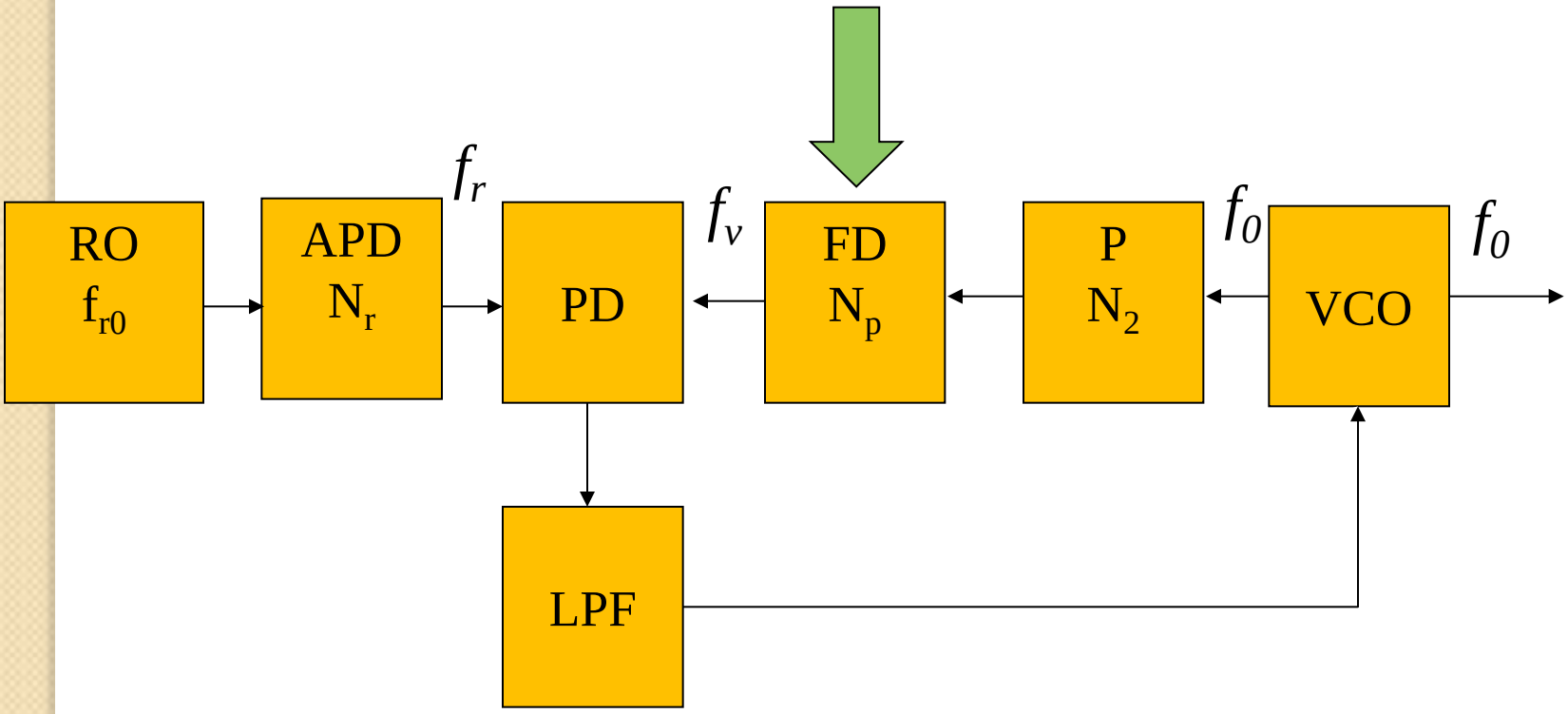


- Performing a phase modulation



Examples of synthesizers using PLL circuits:

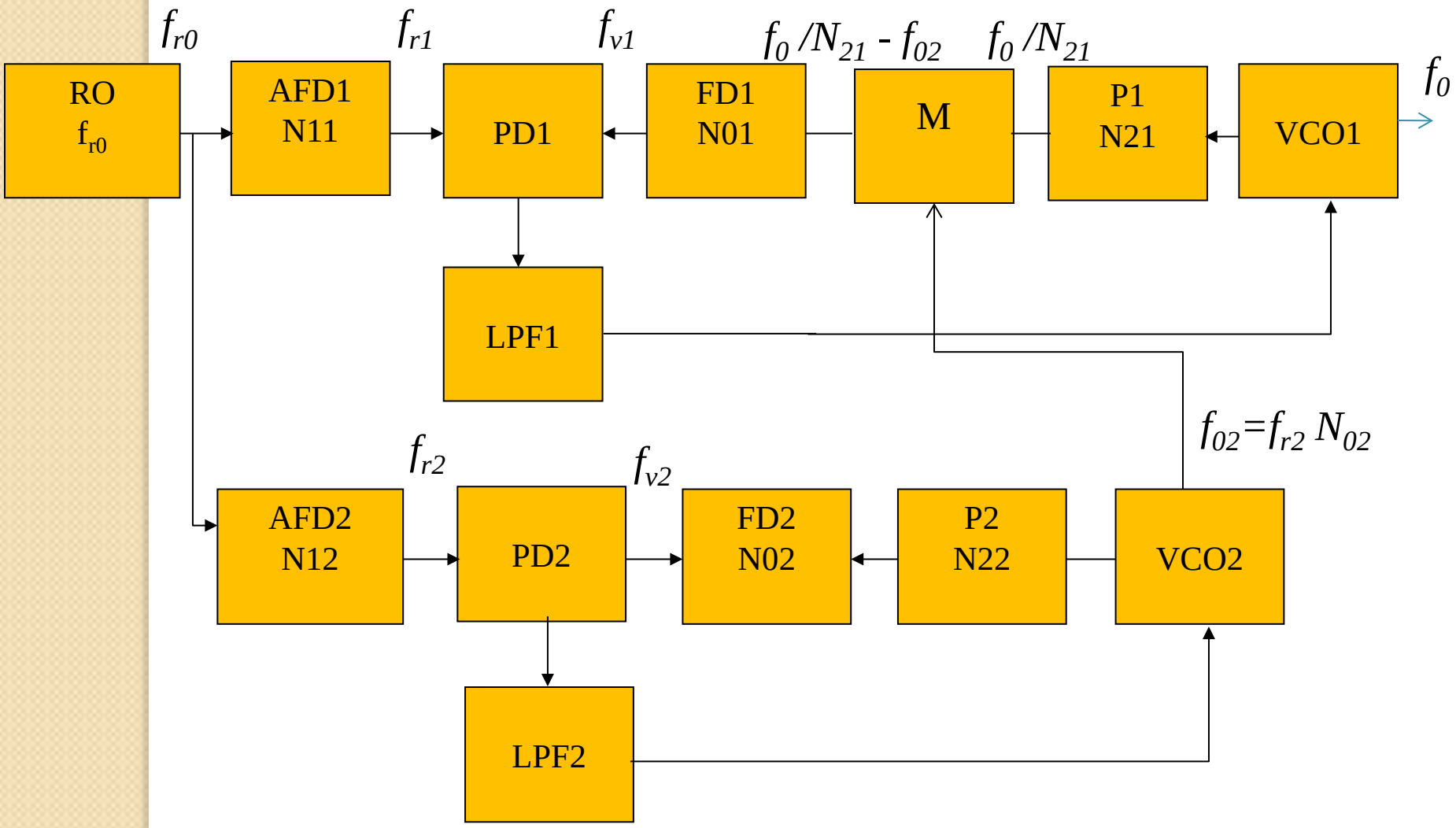
1. *A synthesizer in the range of 300..600 MHz, with a resolution of 100 kHz, settling time of 100 μs, undesired components -80 dBc, phase noise -80 dBc;*



$$f_o = N\, f_r \qquad N = N_2^1 N_P + (N_2^2 - N_2^1) N_A$$

- f_{r0} =1MHz; N_r=10; f_r=100kHz;
- N_P=300..600; N_2=10/11

2. *We require a synthesizer in the range of 4..5 GHz, with a resolution of 1 MHz, settling time of 1ms, undesired components -80 dBc, phase noise -80 dBc;*


f_{r0}
f_{r1}
f_{v1}
$f_0 /N_{21} - f_{02}$
f_0 /N_{21}
f_0
RO
f_{r0}
AFD1
N11
PD1
FD1
N01
M
P1
N21
VCO1
LPF1
$f_{02}=f_{r2} N_{02}$
f_{r2}
f_{v2}
AFD2
N12
PD2
FD2
N02
P2
N22
VCO2
LPF2

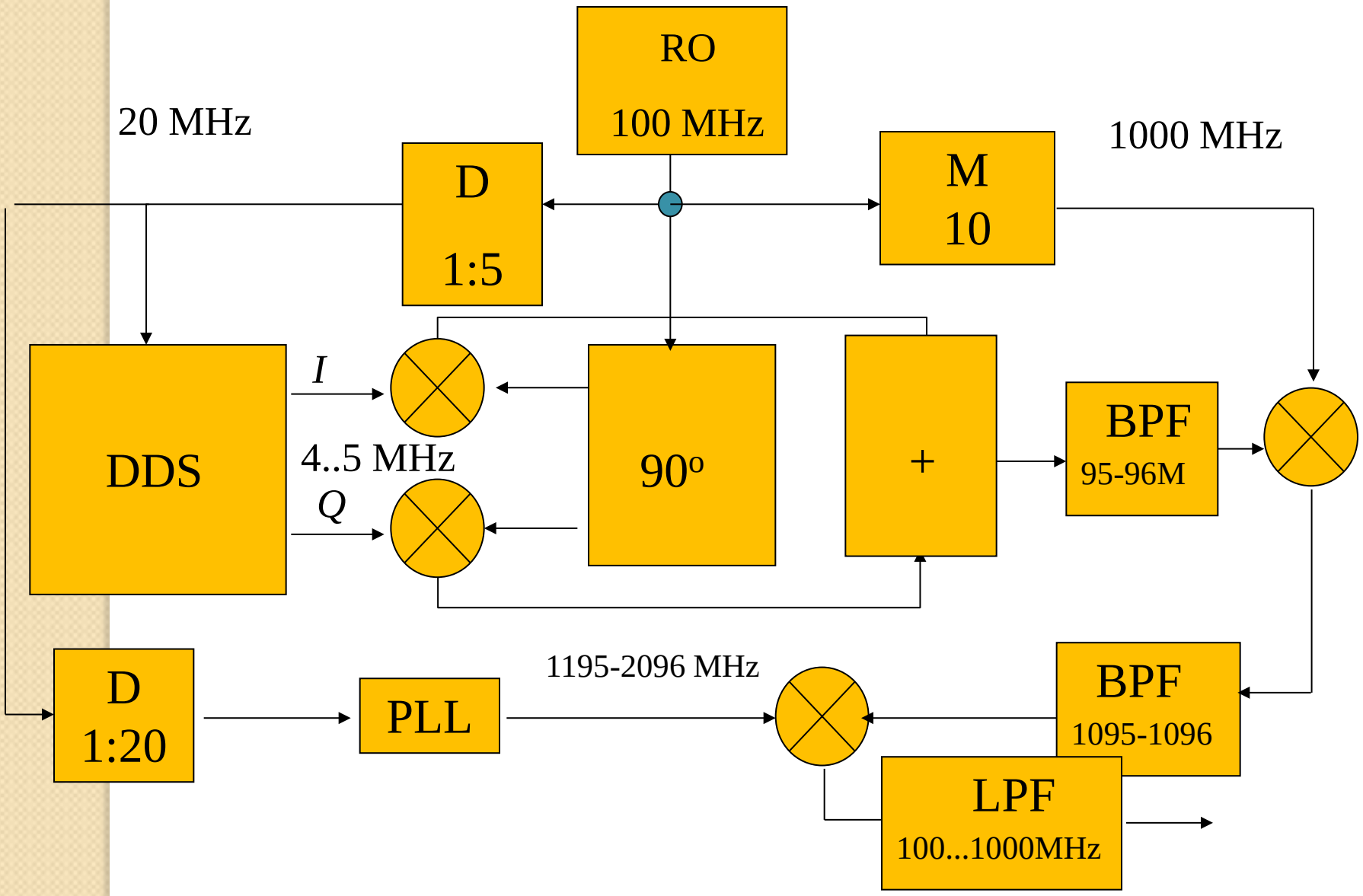
$$f_{o2} = N_{02} f_{r2}; \qquad f_{o1} = (N_{01} f_{r1} + f_{o2}) N_{21}$$

$$f_{o1} = N_{21}(N_{01} f_{r1} + N_{02} f_{r2})$$

$$f_{r1} = \frac{f_{ro}}{N_{11}}, \quad f_{r2} = \frac{f_{ro}}{N_{12}}; \quad f_{r0} = 1MHz$$

	N_1	f_r (kHz)	N_{0min}	N_{omax}	N_2
Main loop (1)	1	1000	28	37	100
Auxiliary loop (2)	100	10	1200	1300	1

3. *A synthesizer in the range of 0.1..1 GHz, resolution of 1 Hz, settling time of 10 μs, undesired components -70 dBc, phase noise - 80 dBc is required;*


RO
100 MHz
20 MHz
D
1:5
M
10
1000 MHz
DDS
I
4..5 MHz
Q
90º
+
BPF
95-96M
D
1:20
PLL
1195-2096 MHz
BPF
1095-1096
LPF
100...1000MHz